# HARDWARE METHODS TO INCREASE EFFICIENCY OF ALGORITHMS FOR DISTRIBUTED LOGIC SIMULATION (Annotation)

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Project verification is an important design stage in creating of electronic devices. The state-of-the-art projects of digital systems are complex and vast. They demand effective resources for verification.

Simulation is used for the functional and timing project simulation. It is run for an error detection on a design stage.

Verification methods with simulation are characterized by heavy timing costs and a sequential execution way of operations. A prospective direction is a parallelization of simulation algorithms. A high performance and non complex parallel or distributed software and hardware for simulation are actual scientific and technical problems.

The subject of research is methods of hardware implementation of synchronization algorithms for a distributed logical simulation. The main idea is a creation of a structural model from a set of functional units. This provides equivalent mapping algorithms for a computational processes and data processing operations.

The combine synchronization algorithm is discussed. The main advantage of this algorithm is a possibility of switching of behavior from optimistic to conservative and vice-versa. A user can configure a behavior of logical processes both automatically and manually. An optimistic logical process will switch if it rollbacks too often, and a conservative logical process will switch if it blocks too often.

A structural implementation of this algorithm is offered. It is a specialized processor for a distributed logical simulation, DESP (Distributed Event-driven Simulation Processor). This device can be implemented using FPGA technology.

The simulation system consists of the specialized workstations. They are joined in a local area network or using a web-interface. Each workstation contains the DESP which can be implemented as a expansion card for a personal computer.

Special software is needed for operating of the simulation system. The architecture of the program system is discussed in the presentation. The simulation process is performed in the following way.

First, a HDL (hardware design language) project is converted to a graph netlist. Next, the obtained graph is cut on separate sections. Each section is assigned to a single logical process. The DESP corresponds to a logical process in a simulation algorithm.

A software data communication subsystem is presented. It transforms a simulated section to a form which is necessary to load in the DESP. During simulation it provides data exchanges with DESP and other workstation in the network.

This paper presents a hardware method to increase efficiency of algorithms for distributed logical simulation. A structural implementation of a combined time synchronization algorithm is offered. The algorithm with dynamic synchronization of calculations is used.

Existed software simulation systems for distributed logic simulation can be extended using the offered method.

The synchronization protocol and its hardware implementation can increase efficiency of distributed logic simulation.