

Concurrent Simulation of Healthy and Faulty Pseudo-boolean Circuits

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The parallel iterative method $X = M \otimes F(X)$ in discrete approximations of electronic circuits is proposed, where X is the vector of signals in the circuit nodes, M is the # operation in the pseudo-Boolean algebra $L_{n,p}^*$, and F is the transformation function defined by a set of Boolean equations.

Keywords: concurrent simulation, switch level, discrete approximation, MOS-transistor.

Logic simulators are of particular importance in large digital circuit design. However the traditional simulators of the gate type exclude direct models of transistor switches, loading transistors, and other similar elements. Alternatively, the analogue circuit simulation programs, like SPICE and MICROCUP, capable of simulating all the types of MOS-circuits in terms of electric circuit parameters, require a large volume of computations even in the analysis of the middle-scale integration circuits. In this situation the class of simulation programs is used on the switch level [1–3]. The simulators on the switch level use transistor structures as elementary basic components and represent the circuit behaviour in the form of a compact set of discrete values. Owing to this, they are capable of analyzing more complicated circuits than the analogue circuit simulation programs.

Pseudo-Boolean circuits, on the one hand, can be considered as the generalization for the logic circuits based on Boolean algebra, and on the other hand, they are discrete approximations of electric circuits in which the parameters such as voltage, current, charge, and capacitance are represented by a finite closed set of values [3]. The concepts of current bidirectivity, Kirchhoff's laws and the superposition principle, take place on the switch level and can be used for determination of the mechanism of pseudo-Boolean signal behaviour. The pseudo-Boolean circuits occupy the place between classical electric circuits and logic ones [3]. The classical Boolean logic circuits of relay-contact and gate devices, the circuits with tristable and wired logic and with open collector elements, are examples of

pseudo-Boolean circuits. Signal S in the pseudo-Boolean circuit has the form $S = (H, G)$, where $H = (H_1, H_2, \dots, H_n)$ can be called the signal force, and $G = (G_1, G_2, \dots, G_n) \in (0, 1, Z, U)$ — the signal state, where 0 (1) is the logical zero (unity) for the voltage levels, and $U (Z)$ are the symbols of indefinite (high-impedance) voltage values. The signal force can be interpreted as current, resistance or conductance. Only two resistances are found in the classical switching networks: $r_0 = 0$ (closed switch) and $r_n = +\infty$ (open switch). To provide more precise estimation of signals, we introduce the fixed number of $n - 1$ additional finite nonzero resistances r_1, r_2, \dots, r_{n-1} , where $r_{i+1} > r_i$. According to set $r = (r_0, r_1, \dots, r_n)$, from Ohm's law $i_k = V/r_k$, we can obtain the totality of discrete current electric forces $I = (i_0, i_1, \dots, i_n)$. We quantify the capacity by $p + 1$ discrete values $C = (c_0, c_1, \dots, c_n)$, where $c_{i+1} > c_i$. The values of c_i can be weighed in voltage levels and, consequently, can be organized into the set $L_1 = \{0, 1, U, Z\}$.

Assume that R current-voltage signals $(v_1, i_1), (v_2, i_2), \dots, (v_R, i_R)$ are applied to node P , the signal value in node P is (v, i) , and it should be the member of L_n . To obtain the signal (v, i) , current, Kirchhoff's current law requires the applied signal currents to be summed, i.e.

$$i = \sum_1^R i_j. \quad (1)$$

Replace (1) by approximation $i = \max_j \{i_j\}$, and from this follows that i is the most strong input signal, $i \in I$. This approximation can be considered as the discrete analogue of Kirchhoff's node current law for pseudo-Boolean circuits. The voltage component v for node P is determined as follows. Let $V = (v_1^j, v_2^j, \dots, v_n^j)$ be the set of voltages of signal pairs with the largest current value, i.e. the pairs (v_k^j, i_k) , for which $i_k = \max_j \{i_j\}$. We define v using the rules: 1) $v = U$ if $U \in V$ or $0, 1 \in V$; 2) $v = 0$ if $0 \in V$ and $1, U \notin V$; 3) $v = 1$ if $0, U \notin V$; 4) $v = Z$, if $0, 1 \in V$.

The rules of computation of (v, i) described above can be expressed by the $\#$ operation considering as lattice L_n [2,3]. The connection operator $\#$ is the lowest upper bound operator (lub), whose use gives $(v, i) = \#((v_1, i_1) \dots (v_m, i_m))$. L_n is the $(3n + 1)$ -valued pseudo-Boolean algebra with zero $\{z, r_n\}$ and unity $\{U, r_0\}$. The lattice operation \cup is equivalent to connection operator $\#$ defining the signal voltage interaction at the node. If resistors and capacitances with $n + 1$ and $p + 1$ different values are connected into the pseudo-Boolean circuit, then the corresponding algebras L_n and L_p^* are combined into the algebra $L_{n,p}$ which represents $(3(n + p - 1) + 1)$ -valued pseudo-Boolean algebra.

Let y_i be the external input node or the capacitance source. If there exists an unblocked path without loops connecting v and y_i , then the signal at the node v is the lowest upper bound (lub) y_i : $\text{val}(v) = \text{lub}\{y_i\}$ [1,4]. Let the signal value at node u be

$S_u = (H_u, G_u)$. If the component of type T connects nodes v and u and has the value R at its gate, then we can determine function $f(T, R, H_u, G_u)$ — i.e. the function of transformation of signal u into v . For each node v its new signal value S_u^j is the sum of functions $f(T, R, G_u, H_u)$ ($\{u\}$ are the neighbours of node v) and the past capacitance value for v [4]. To determine the stable state of the circuit, the computations continue until $S^{(i+1)}$ is equal to $S^{(i)}$. The Bryant algorithm is the modification of this computation procedure [4].

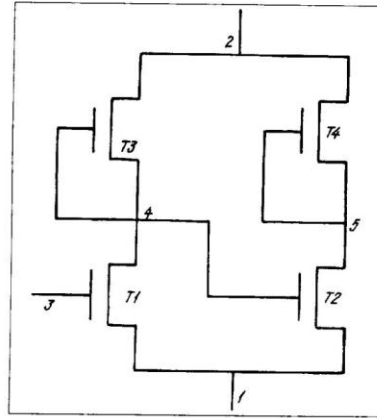


Figure 1. The circuit consisting of two inverters.

The interaction of multivalued signal components in the circuit node

can be represented by the appropriate set of Boolean equations. These equations describe the component behaviour as a one-way direction device. Their actual two-way direction is represented in the data structures. The description of the pseudo-Boolean circuit contains the following data structures:

$Q_1, Q_2, Q_3, T = (T_1, T_2)$. The dimension of every array is $L = \sum_{i=1}^N k_i$, where k_i is the number of the neighbours of node i , N is the number of circuit nodes; $Q_1[k]$, $Q_2[k]$ and $Q_3[k]$ are the numbers of drain, source, and gate of the node which has type $T[k]$. For example, the circuit consisting of two inverters (see Fig. 1) is characterized by structures $Q_1 = (1, 2, 3, 4, 4, 5, 5)$, $Q_2 = (2, 2, 2, 3, 4, 4, 5)$, $Q_3 = (1, 2, 3, 1, 2, 1, 2)$, $T_1 = (1, 1, 1, 1, 0, 1, 0)$ and $T_2 = (1, 1, 1, 1, 0, 1, 0)$.

Assume that $n + 1$ types of attenuators, $p + 1$ types of sources, and p -MOS and n -MOS transistors are connected into the pseudo-Boolean circuit. The finiteness of the number of signal converters (transistors, resistors, and capacitors) and the finiteness of the set of signals being used, provide the principal possibility of expressing the relations between the signal components for each type of converter and then for the whole circuit using the Boolean relationships. Number the MOS-structure elements as follows: n -MOS and p -MOS transistors have numbers 0 and 1, respectively; attenuators $r_0, r_1, r_2, \dots, r_{n-1}$ have numbers 2, 3, ..., n ; capacitances $c_0, c_1, c_2, \dots, c_{p-1}$ have numbers $n + 1, \dots, n + p$. Denote the type of element (or its number from 0 to $n + p$) as the Boolean vector $T = (T_1, T_2, \dots, T_m)$, where m is the least integer number, not less than $\log_2(n + p + 1)$. Let the Boolean functions for attenuators $D_i^r(T)$ be equal to unity if the attenuator is the i -th type, and be equal to

zero — otherwise, for $i = 0, n + p$. The similar functions $D_j^c(T)$ are equal to unity for the capacity of type j , and zero — otherwise, for $j = 0, p - 1$. The corresponding functions for transistors are denoted as D^0 and D^1 .

The operation of n -MOS transistor can be described in the following way: $f(T, R, H, G) = Z$, if $D^0 = 1$ and $R = 0$, and $f(T, R, H, G) = (H, G)$ if $D^0 = 1$ and $R = 1$. For p -MOS transistor the expressions are similar: $f(T, R, H, G) = Z$ if $D^1 = 1$ and $R = 1$, and $f(T, R, H, G) = (H, G)$ if $D^1 = 1$ and $R = 0$. The signal transformations by the attenuators r_1, r_2, \dots, r_{n-1} can be represented by the matrix $r_{i,k}$ with dimension $(n + p) \times n$ in which the k -th column contains the signal values from r converted by attenuator r_k . For each $k = 0, n - 1$ we can write $f(T, R, H, G) = (r_{i,k} G)$ at $H = r_i, D_k^r = 1$ for $i = 0, n - 1$, and $f(T, R, H, G) = (c_{j,k}, G)$ at $H = c_j, D_k^r = 1$ for $j = 0, p - 1$. From $i < j$ it follows $r_{i,k} \leq r_{j,k}$, and if $k < l$, then $r_{i,k} \leq r_{i,l}$.

The source (capacitance) behaviour for the i -th type ($i = 0, p - 1$) can be determined by the expression $f(T, R, H, G) = (c_i, GQ)$ if $D_i^c = 1$, where CQ is the previous node state. The signal logic force can be determined as follows

$$A_i^r = \bigvee_{k=1}^{n-1} r_{i,k} \left(\bigvee_{m=1,l} H_m \oplus r_{i,k}^m \right); \quad A_i^c = \bigvee_{k=1}^{p-1} c_{i,k} \left(\bigvee_{m=1,l} H_m \oplus C_{i,k}^m \right),$$

where $H_m, r_{i,k}^m$ and $c_{i,k}^m$ are the m -th components of values $H, r_{i,k}$ and $c_{i,k}$, respectively; \oplus is the "EXCLUSIVE OR" operation (sum to modulo 2).

Let be $F = f(T, R, H, G)$, and then for bit components $F = (FH, FG)$, $FH = (FH_1, FH_2, \dots, FH_i)$, and $FG = (FG_1, FG_2, FG_3)$, using the notation chosen and assuming that $R = (R_1, R_2, R_3)$, $H = (H_1, H_2, \dots, H_i)$, and $G = (G_1, G_2, G_3)$, we can obtain the following expressions

$$FH = HE(R) D^0 \bigvee_{i=1}^{n-1} H\bar{E}(R) D^1 \bigvee_{i=1}^{n-1} D_i^r A_i^r \bigvee_{i=1}^{p-1} D_{i+n+1}^c A_i^c \bigvee_{i=0}^{p-1} D_i^c CQ_i; \quad (2)$$

$$FG = GE(R) \bar{D}^0 \bigvee_{k=0}^{n-1} GE(R) D^1 \bigvee_{k=0}^{n-1} G \left(\bigvee_{k=0}^{n-1} D_k^r \right) \bigvee_{i=0}^{p-1} GQ \left(\bigvee_{i=0}^{p-1} D_i^c \right) \quad (3)$$

where $E(R) \bar{E}(R)$ are the Boolean functions equal to unity at $R = 1(0)$.

We can compute any component of multivalued signal of all circuit nodes simultaneously (because it is given by the Boolean equations (2) and (3)) using *SIMD*-computers.

Consider 13-valued pseudo-Boolean algebra $L_{2,3}$ including signals $\{Z, (C0, C1), CX, (SC0, SC1), SCX, (W0, W1), WX, (D0, D1), DX\}$ [4]. We use signal coding $Z = (Z_h, Z_g)$, where $Z_h = (0, 0, 0, 0)$, $Z_g = (0, 0, 0, 0)$, $D = (1, 0, 0, 0)$, $W = (0, 1, 0, 0)$, $SC = (0, 0, 1, 0)$, $C = (0, 0, 0, 1)$, $X = (1, 0, 0, 0)$, $1 = (0, 1, 0, 0)$ and $0 = (0, 0, 1, 0)$.

Considering the resistor operation according to the third rule [4], we have $A_1^r = H_1 D \vee H_2 W$ and $A_1^c = H_3 SC \vee H_4 C$.

To code the circuit element types (transistors, resistors), we can use the Boolean vector $T = (T_1, T_2)$. The proper n -MOS transistor is coded as $T_1 = 1, T_2 = 1$ while p -MOS transistor is coded as $T_1 = 1, T_2 = 0$. The loading transistor playing the role of the resistor in the integrated MOS-circuits is coded as $T_1 = 0$. Then $D^0 = T_1 T_2$, $D^1 = T_1 \bar{T}_2, D^2 = \bar{T}_1$. The final equations are of the form

$$\begin{aligned} FG_1 &= G_1 T_1 (\overline{R_2 \oplus T_2}) \vee G_1 \bar{T}_1; \\ FG_2 &= G_2 T_1 (\overline{R_2 \oplus T_2}) \vee G_2 \bar{T}_1; \\ FG_3 &= G_3 T_1 (\overline{R_2 \oplus T_2}) \vee G_3 \bar{T}_1; \\ FH_1 &= T_1 H_1 (R_2 \oplus T_2); \\ FH_2 &= T_1 H_2 (\overline{R_2 \oplus T_2}) \vee \bar{T}_1 H_2 \vee \bar{T}_1 H_1; \\ FH_3 &= T_1 H_3 (\overline{R_2 \oplus T_2}) \vee T_1 \bar{H}_3; \\ FH_4 &= T_1 H_4 (\overline{R_2 \oplus T_2}) \vee T_1 \bar{H}_4. \end{aligned}$$

The signal values for the working fields in the given circuit are shown in Table 1. The multicomponent working fields $S^0, R, (H, G), F$ of the multivalued signal values at the device nodes correspond to Q_1, Q_2, Q_3 , and the transformation function f , respectively.

Table 1

Iteration	Field name	Node values at the field								Iteration	Field name	Node values at the field							
1	S^0	D0	D1	D1	CX	CX	CX	CX	2	S^0	D0	D1	D1	D0	D0	W1	W1		
	R	1	1	1	1	X	X	X		R	1	1	1	1	0	0	1		
	H,G	D0	D1	D1	D0	D1	D0	D1		H,G	D0	D1	D1	D0	D1	D0	D0		
	F	D0	D1	D1	D0	W1	Z	W1		F	D0	D1	D1	D0	W1	Z	W1		

The analysis of defects in the MOS-circuits shows that most can be simulated by the faults of type "stable open-circuit of a transistor" (SOP) and "stable shorting of a transistor" (SON) [5]. The first take the circuit from the combinatorial circuit class to the sequential circuit class, the second are responsible for the unstable output signals. The transistors which are added into the healthy device to simulate the different kind faults are described in [6, Fig. 9.5]. The simulation of the healthy circuit and the circuits with these types of faults reduces to the simulation of the circuit with the added transistors with nonactive (active) gates of those transistors, respectively. The arrays Q_1, Q_2, Q_3, T can be easily modified for simulation of the faults such as source-drain short-circuiting, gate open-circuiting, and so on.

Thus the logic many-valued simulation of pseudo-Boolean devices is surveyed with the use of parallel iterative method $X = M \oplus F(X)$, where M is the operator *tub*, and F symbolizes the parallel computations associated with Boolean equations (2), (3). The emulation of Boolean SIMD-computations for F is feasible with the help of functions *putimage* and *getimage* of the C programming language on an IBM PC.

When employing the above functions for operations with IBM PC video memory, the simulation time for the circuits consisting of 1179, 2979, 7107, 12771, and 20938 transistors in the $L_{2,3}$ alphabet for ten input sets comprised 10, 25, 60, 110, and 170 s, respectively. The average number of iterations is 15. The simulation was performed on an IBM PC AT/386 with the clock rate of 40 MHz.

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