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10th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

Kharkov, Ukraine, September 14-17, 2012

The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
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- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics http://anpre.org.ua/ in cooperation with Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Trades Committee of Kharkov National University of Radioelectronics and Trades Committee of Students, Aldec, Synopsys, Kaspersky Lab, DataArt Lab, Tallinn Technical University.

CONTENTS

Compositional Microprogram Control Unit with Operational Automaton of Transitions

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Abstract

The using of operational automaton of transitions as the block of microinstruction addressing of compositional microprogram control unit is proposed. The new structure model of compositional microprogram control unit with reduced hardware amount is developed. The generalized structure of operational automaton of transitions is suggested. An example of process of synthesis of compositional microprogram control unit with operational automaton of transitions is given.

1. Introduction

A control unit is used in a vast majority of digital systems [1]. Nowadays, we witness the tremendous growth for the complexity of problems to be solved by digital systems. It requires development new, more effective methods for synthesis of control units. One of the most important problems in this area is the development of design methods leading to decreasing the cost of a resulting system.

If a control algorithm of a digital system is represented by a linear graph-scheme of algorithm (GSA), then the model of compositional microprogram control unit (CMCU) [2] can be used for implementing the corresponding control unit. A CMCU can be viewed as a composition of automata with "hardwired" and "programmable" logic. The overwhelming majority of transitions in CMCU are executed using a counter. But transitions depended on logical conditions are executed using a combinational circuit having irregular nature [2]. The methods of CMCU's synthesis are based on constructing so-called operational linear chains (OLC). The transitions within the same OLC are executed using the counter. The transitions between different OLCs are executed using special block of microinstruction addressing (BMA).

There are many approaches leading to decreasing the hardware amount (logical gates quantity) in logic circuit of BMA. As a rule, these methods are based on multilevel organization of BMA [3, 4]. But these methods result in decreasing for performance of CMCU. For many practical tasks, the performance of digital system should be as high as possible. So, the methods of multilevel organization can't be used here.

The authors proposed a design method for reduction of hardware amount in the logic circuit of finite-state machine (FSM) [5]. It is based on usage of a special operational automaton of transitions (OAT) for generating codes of next states. In this article we propose using this approach for CMCU. It can result in decreasing the hardware amount in comparison with known methods of CMCU design.

2. Organization of CMCU with operational automaton of addressing

The base model of CMCU is shown in Fig. 1. Let us denote this model as U_1.

In CMCU U_1, the block BMA and register RG form an FSM S1. It executes transitions between outputs and inputs of OLCs in line with the following system

$$\Phi = \Phi (\boldsymbol{\tau}, X). \qquad (1)$$

In the system (1), the set $\boldsymbol{\tau}$ includes logical variables $\tau_r \in \boldsymbol{\tau}$ used for encoding states $b_m \in B$, where $B=\{b_1, ..., b_{Mo}\}$ is a set of states of FSM S1. The number of variables in $\boldsymbol{\tau}$ is determined as

$$R_B = \lceil \log_2 M_o \rceil. \qquad (2)$$

The second component of the equation (1) is the set of logical conditions $X=\{x_1, ..., x_L\}$. Each conditional vertex of GSA Γ contains one element of X. The transitions between states of FSM S1 are determined by the system

$$\Psi = \Psi (\boldsymbol{\tau}, X). \qquad (3)$$

Let us point out that $|\tau| = |\Psi| = R_A$ and $|\Phi| = R$. The value of R is determined as

$$R = \lceil \log_2 M \rceil. \qquad (4)$$

In (4), the value M is equal to the number of operator vertices in GSA Γ (it is the same as the number of microinstructions kept into the control memory).

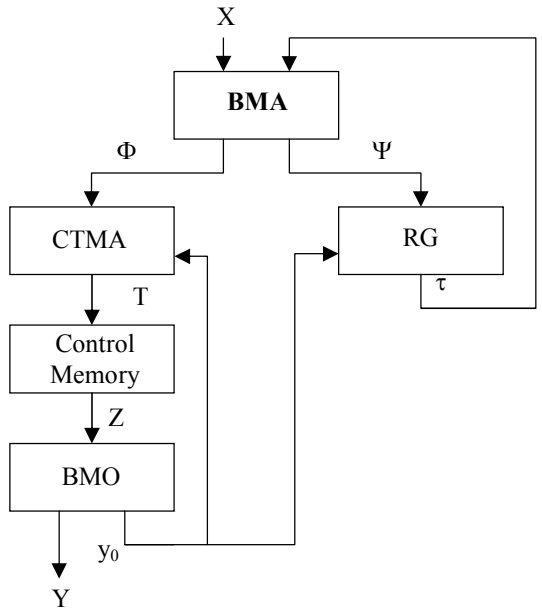

Figure 1. The base model of CMCU

The counter of microinstruction address (CTMA), the control memory (CM) and the block of microoperations (BMO) form a microprogram control unit (MCU) S2 with natural addressing of microinstructions [6]. The MCU S2 executes transitions between microinstructions corresponding operator vertices from the same OLC. Such a transition is executed by incrementing the CTMA's content due to variable y_0=1. The block BMO is used for generating microoperations $y_n \in Y$, where $Y=\{y_1, ..., y_N\}$ is a set of microoperations. The BMO is necessary if some method of encoding of collections of microoperations is used [6]. The BMO generates also a variable y_0. If y_0=1, then the FSM S1 does not change its state and addressing of microinstructions is executed by CTMA. If y_0=0, then the output of some OLC is reached. In this case, the FSM S1 generates new values of functions (1) and (3) and a transition between outputs and inputs of OLCs is executed.

The drawback of CMCU U_1 is an irregular structure of logic circuit of BMA [2]. It is implemented using such "small" elements as, for example, LUT elements of FPGA [7]. We propose using standard operational blocks (OB) such as adders, shifters and so on for implementing BMA. These blocks are standard library elements of CAD systems [8, 9] and their circuits are optimized. Usage of standard blocks leads to decreasing the design time and increasing the reliability of resulting projects.

Let us introduce an operational automaton of transitions (OAT) in CMCU U_1. In this case the system (3) includes both arithmetical and logical operations. It leads to CMCU U_2 shown in Fig. 2.

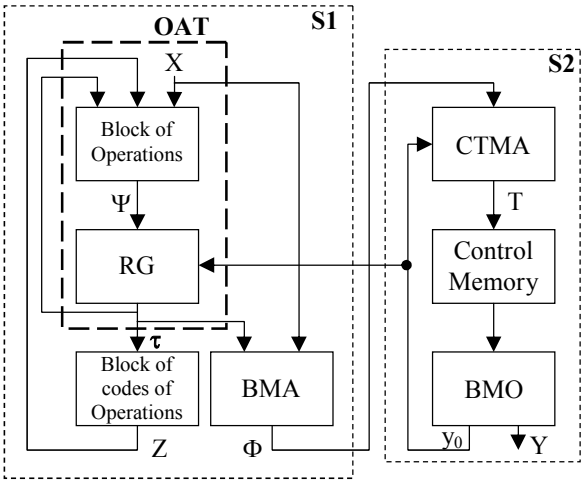

Figure 2. Structure diagram of CMCU U_2

The block BO has the following structure (Fig. 3).

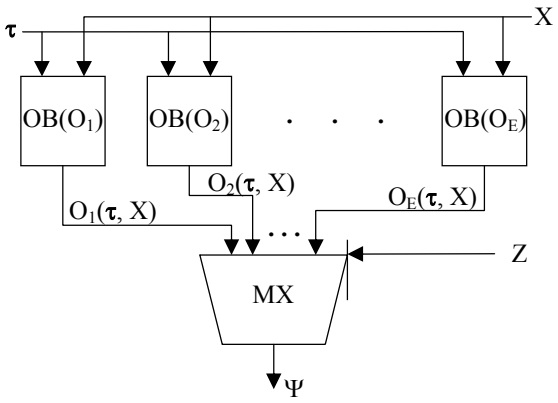

Figure 3. Structure diagram of block of operations

In BO, the symbol $OB(O_e)$ stands for the operational block executing some operation $O_e \in O$ ($e = \overline{1, E}$). The symbol $O_e(\tau, X)$ means the outcome of operation $O_e \in O$. The multiplexor MX is used for

transferring the proper code to form correct values of the functions Ψ. The choice is determined by variable $z_r \in Z$ from BCO.

The proposed method can be used if the total hardware amount in the circuit of S1 for CMCU U_2 is less than for its counterpart from U_1. This fact can be proved either by results of design for both U_1 and U_2 or by some formula. These problems are beyond the scope of this article.

4. Investigation of CMCU with OAT

Let us use the minimum hardware amount as an efficiency criterion for CMCU U_2. Let us find the efficiency E_{U_2} of CMCU U_2 in comparison with CMCU U_1 as the following relation:

$$E_{U_2} = \frac{H_{U_1}}{H_{U_2}}. \qquad (5)$$

In (7), H_{U_1} is a hardware amount in logic circuit of BMA in CMCU U_1 used for implementing the system (3); H_{U_2} is a hardware amount in logical circuit of OAT in U_2. Obviously, if there is $E_{U_2} > 1$, then CMCU with OAT needs less amount of hardware than CMCU U_1.

According to our investigations, the next generalized dependences of hardware amount are discovered:

$$H_{U_1} = H_1(R, R_{LC}, T, k_1), \qquad (6)$$

$$H_{U_2} = H_2(R, R_{LC}, T, k_2). \qquad (7)$$

In (8) and (9), the following symbols are used:

R is the number of bits of address of microinstruction;

R_{LC} is the average number of logical conditions analyzed in the same transition;

T is the number of transitions in GSA (equal to the number of conjunctive terms in system (3) for CMCU U_1);

k_1 is a coefficient of minimization of complexity for the equations of system (3) for structure U_1 due to the usage of some standard optimization methods of Boolean equations ($k_1 = \overline{0,1}$);

k_2 is a coefficient defined as relation of the average hardware amount for one OT in CMCU U_2 to hardware amount required for one term in system (3) in CMCU U_1.

According to (5)-(7), several dependences of E_{U_2} from these parameters are obtained by the authors. Let us overview some of them for the following values: R=10, R_{LC}=2, T=2000, k_1=0,8, k_2=30.

The function $E_{U_2}(T)$ is shown in Fig. 4. As follows from Fig. 4, this function is linear. The CMCU U_2 becomes more effective when there is T>800. The further growth of the number of transitions leads to the growth of the gain.

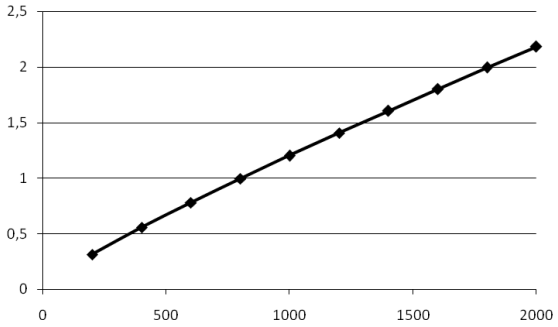

Figure 4. Dependence $E_{U_2}(T)$

The function $E_{U_2}(R)$ is shown in Fig. 5. Analysis of Fig. 5 shows that this function is restricted by the value 2,05. So, the logic circuit of CMCU U_2 always needs less hardware then the logic circuit of CMCU U_1.

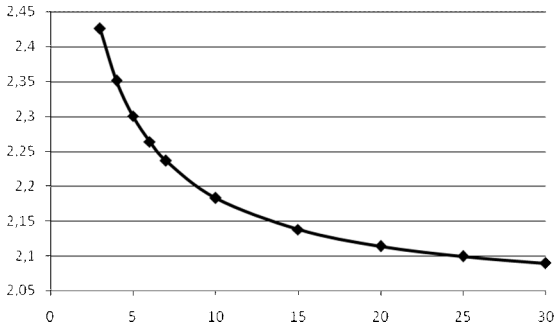

Figure 5. Dependence $E_{U_2}(R)$

We do not show the function $E_{U_2}(k_1)$ because of its linear nature. If k_1=1 (no minimization is possible), then E_{U_2} reaches its maximum value equal to 2,73. Only in the case when usage of minimization simplifies the system (3) up to 60% (reducing up to 40% of logical gates), the application of CMCU U_1 makes sense.

The function $E_{U_2}(k_2)$ is shown in Fig. 6. As follows from the Fig. 6, the growth of average complexity of operational blocks used for executing transitions leads to decreasing of efficiency E_{U_2}. For values of arguments, our approach can be applied till $k_2<65$.

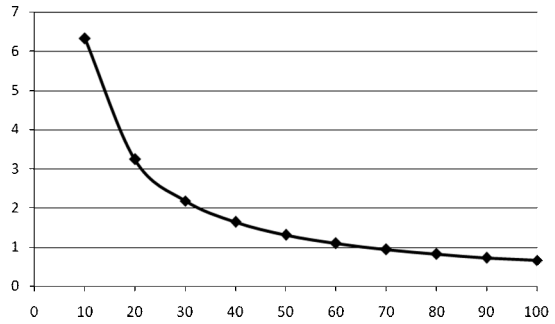

Figure 6. Dependence $E_{U_2}(k_2)$

Analysis of functions shown on Fig. 4 – Fig. 6 allows determine the main factors providing increase for efficiency of CMCU U_2: the growth of number of transitions, the decrease the length of address of microinstruction, and the implementing control algorithms with small rate of minimization.

5. Conclusions

In this article we propose using an operational automaton for executing transitions in CMCU. It allows using standard library elements of CAD tools in CMCU design. This approach can decrease the hardware amount because the same operational element can be used for executing a lot of transitions. Also, the process of design is simplified due to use of standard library elements such as adders, shifters, incrementors, multiplexors and so on.

As we can see from achieved experimental results, using the operational automaton of transitions can reduce hardware amount of logical circuit of CMCU by several times in comparison with base model of CMCU.

There are some directions for development of the proposed approach. We should develop a method for constructing the set of operations leading to decrease of hardware amount in the operational automaton of transitions. Next, some optimization method should be developed for further hardware decrease in the logical circuit of CMCU with OAT.

6. References

[1] Baranov S. Logic and system design of digital systems. – Tallinn: TUT Press, 2008. – 266 pp.

[2] Barkalov A., Titarenko L. Logic Synthesis for Compositional Microprogram Control Units. – Berlin: Springer, 2008. – 272 pp.

[3] Wisniewski R. Synthesis of compositional microprogram control units with programmable devices. – Zielona Gora: UZG Press, 2009. – 146 pp.

[4] Barkalov A., Titarenko L. Code conversion in compositional microprogram control units // Cybernetics and System Analysis. V. 47, № 5, 2011. – pp. 763-772.

[5] Barkalov A., Babakov R. Operational formation of state codes in microprogram automata // Cybernetics and System Analysis. V. 47, № 2, 2011. – pp. 193-197.

[6] Barkalov A., Wegrzyn M. Design of Control Units with Programmable Logic. – Zielona Gora: UZ Press, 2006. – 150 pp.

[7] Maxfield C. The Design Warrior's Guide to FPGAs. – New Jersi: Elsevier. – 2004. – 542 pp.

[8] Altera Corporation, 2012. Available at: <www.altera.com>

[9] Xilinx Inc., 2012. Available at: <www.xilinx.com>