A PARALLEL IMPLEMENTATION OF THE INTERSECTION STAGE OF RAY-TRACING ALGORITHM

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Analyses of mathematical expressions for all stages of Ray tracing algorithm show that the main operation is multiplication.

Intersection stage

Parameter t for polygonal model has to be calculated as relation of dividend (dev) to devisor (div)

$$t = -\frac{dev}{div}.$$

To calculate devisor - scalar product of viewpoint vector to normal vector of a plane:

$$\text{div} = S = v_x^o \cdot n_x + v_y^o \cdot n_y + v_z^o \cdot n_z .$$

To calculate parameter *d* for a plane equation:

$$d = -(n_x \cdot x[0] + n_y \cdot y[0] + n_z \cdot z[0]).$$

To calculate dividend:

$$\text{dev} = n_x \cdot x_v^o + n_y \cdot y_v^o + n_z \cdot z_v^o + d.$$

That is why an elementary performing block (EBL) has to realize a multiplication

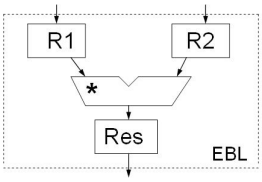

Figure 1. Functional organization of an elementary performing block

Looking to the 1st equation of the system (fig. 1), it needs realization of 3 multiplications and then 3 additions (fig. 2).

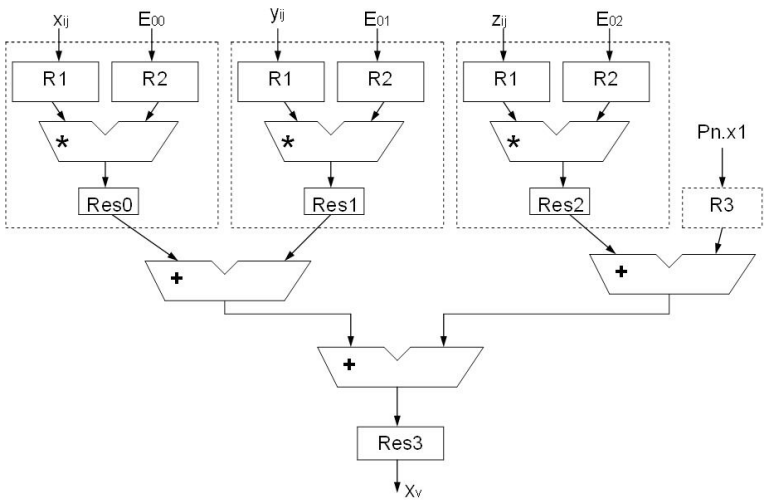

Figure 2. Functional organization of a performing block to calculate X-coordinate of point

Realization of intersection stage by applying of the main performing block.

Looking to the system (fig. 2), we can see that x, y and z coordinates are uncorrelated and can be calculated in parallel (fig. 3).

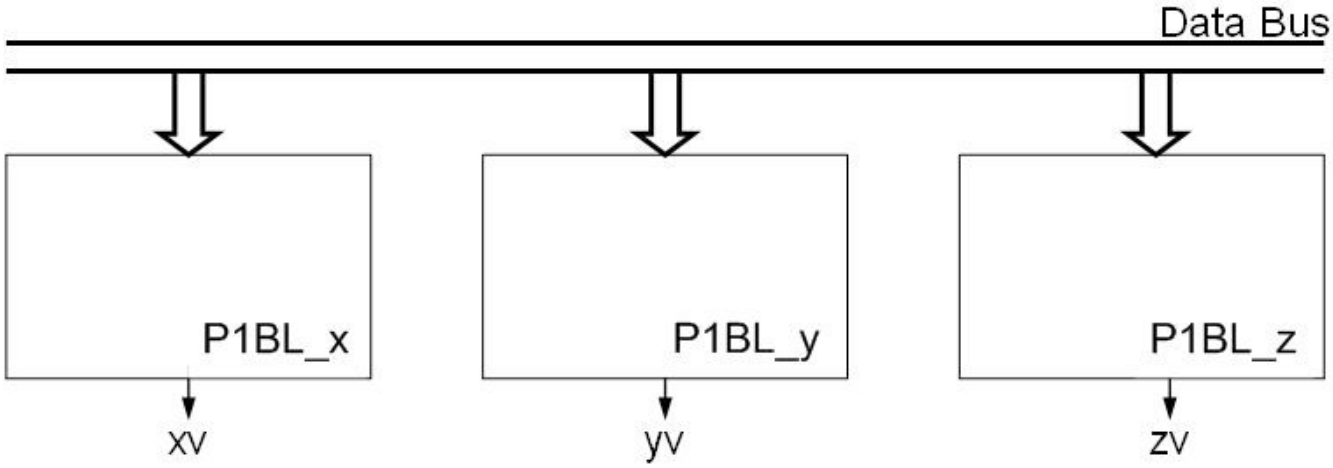

Figure 3. Parallel realization of the system

Application of the main processing block P1BL allows to realize 3 multiplications in parallel. In this case time of 3 multiplications will be equal to 1 tm or 4 processing loops. Application of 3 processing block P1BL in parallel allows to realize 9 multiplications in parallel. In this case time of 9 multiplications will be equal to 1 tm or 4 processing loops. izations.

Table 1. Comparing of processing loops for sequential and parallel realizations

Type of operation	Number of processor loops		
	Sequentially	Using parallel realization	
		P1BL (P0BL)	3 P1BL(P0BL) in //
One Ray parameters calculation			
Multiplication	$29 \cdot t_m$	$10 \cdot t_m$	$4 \cdot t_m$
Addition/subtraction	$26 \cdot t_a$	$9 \cdot t_a$	$7 \cdot t_a$
Intersection stage (for one plane)			
Multiplication	$9 \cdot t_m$	$3 \cdot t_m$	$1 \cdot t_m$
Addition/substruction	$7 \cdot t_a$	$6 \cdot t_a$	$3 \cdot t_a$
Division	$1 \cdot t_d$	$1 \cdot t_d$	$1 \cdot t_d$
Unary minus	$2 \cdot t_-$	$2 \cdot t_-$	$2 \cdot t_-$

Table 1 shows decreasing of processing loops for parallel realizations for scenes' complexity from 100 up to 1000 planes. Application of the main processing block P1BL to realize 3 multiplications in parallel reduces processing time by 46,4%.

Application of 3 processing block P1BL in parallel to realize 9 multiplications in parallel reduces processing time by 66,8%.

Table 2. Numbers of processing loops for sequential execution and for parallel realizations for scenes' complexity from 100 up to 1000 planes

Number of planes	Number of processing loops for sequential execution	Parallel realization			
		P1BL (P0BL)		3 P1BL/P0BL in //	
		Number of processing loops	% of decreasing	Number of processing loops	% of decreasing
100	5542	2949	46,79	1823	67,11
200	10942	5849	46,55	3623	66,89
300	16342	8749	46,46	5423	66,82
400	21742	11649	46,42	7223	66,78
500	27142	14549	46,40	9023	66,76
600	32542	17449	46,38	10823	66,74
700	37942	20349	46,37	12623	66,73
800	43342	23249	46,36	14423	66,72
900	48742	26149	46,35	16223	66,72
1000	54142	29049	46,35	18023	66,71
Average:			46,4		66,8

Figure 4 shows diagrams - comparing of processing loops for sequential and parallel realizations.

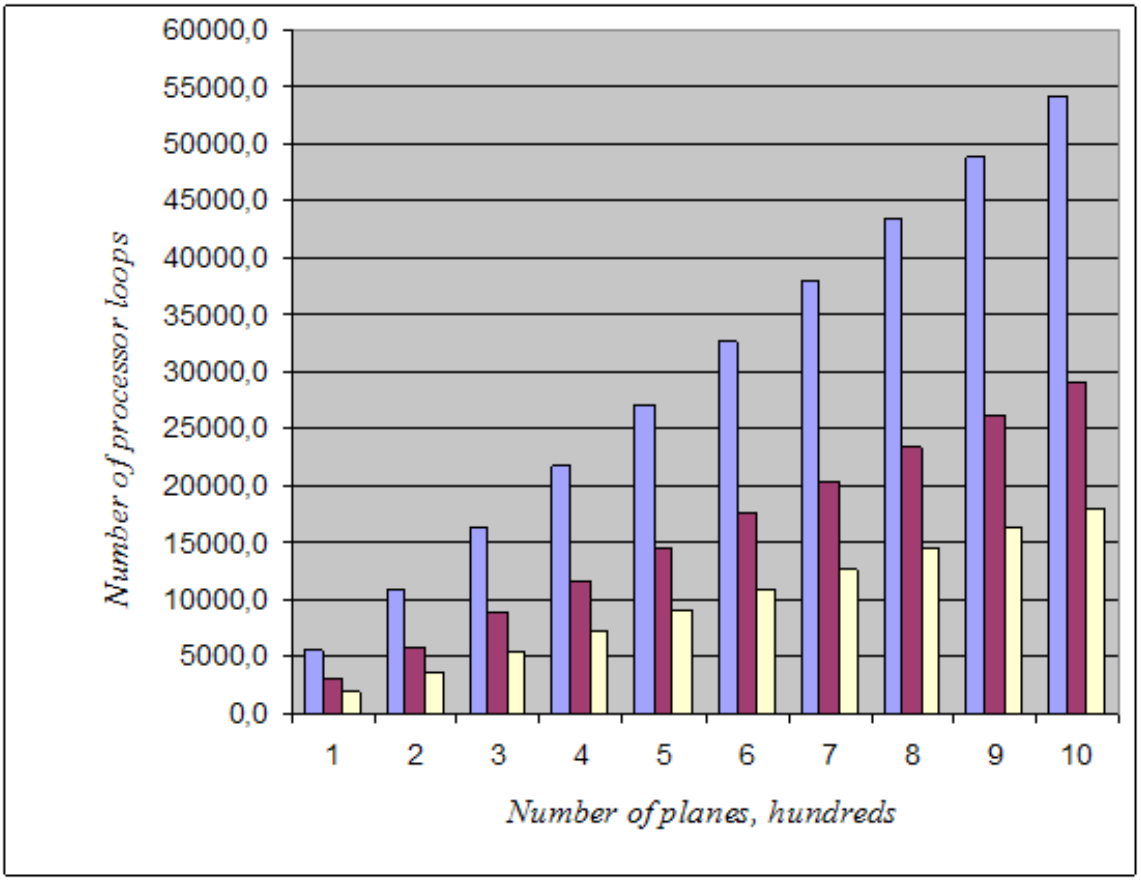

Figure 4. Comparing of processing loops for sequential and parallel realizations

Summaries

To improve system performance the parallel realization of intersection stage is proposed. For this aim structure of an elemental block is used. The main performing block are developed. Implementations of the systems and expressions show that minimum processor unit has to construct 3 parallel performing block P1BL with reconfigurable structure.Application of the main processing block P1BL to realize 3 multiplications in parallel reduces processing time by 46,4%. Application of 3 processing block P1BL in parallel to realize 9 multiplications in parallel reduces processing time by 66,8%.

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