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CONTENTS

Modification of Elementary Operational Linear Chains in Compositional Control Unit with Code Sharing

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***Abstract* – The new design method for compositional microprogram control units with code sharing and elementarization of operational linear chains is proposed. The method targets on reduction in the number of LUT-elements in the combinational part of control unit. Some additional control microinstructions containing codes of the classes of pseudoequivalent chains are used for operational linear chains modification. Proposed method is illustrated by an example. Most desirable GSA characteristics for using proposed method were obtained.**

***Index Terms* – Circuit synthesis, flow graphs, logic devices, minimization methods.**

I. Introduction

Using of any elementary basis for realization of control unit circuits causes necessity of taking into account not only control algorithm peculiarities but basis features also. The task of hardware amount decrease became very urgent when one need to realize complex of operational and control units on one chip [1]. One of possible way of this task solving is hardware amount decrease in control unit due to using of pseudoequivalent states of Graph-Scheme of Algorithm (GSA). High percentage (>75%) of operational vertices in GSA [2] and presence of embedded memory blocks make it possible of using this synthesize method modification.

Compositional microprogram control unit (CMCU) is reasonable to use in case of linear GSA (percentage of operational vertices in GSA is over 75%) [2]. FPGA (Field-Programmable Gate Arrays) basis is commonly used for realization of control unit circuit [3, 4]. Modification of synthesis method for CMCU with code sharing and modification of operational linear chains (OLC) is proposed in this article.

The main purpose of investigation is simplification of combinational part of CMCU via implementation to GSA of additional vertices containing pseudoequivalent operational linear chain (POLC) class code. The main task of investigation is development of CMCU synthesis method modification that let decrease number of LUT-elements (Look-Up Tables, structural elements of FPGA basis) in Block of Microinstruction Addressing (BMA). Control algorithms are represented as GSA.

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II. Main Statements

Graph-scheme of control algorithm consists of operational and conditional vertices, making sets E_1 and E_2 accordingly, and the set of arcs E. Let us begin vertex be marked as b_0, end – b_E. Operational vertex $b_q \in E_1$ contain set of microinstructions $Y(b_q) \subseteq Y$, where $Y = \{y_1,...y_N\}$ is the set of output signals of control unit. Conditional vertex $b_g \in E_2$ contains one elements $X(b_g)$ of the logical conditions set $X = \{x_1,...x_L\}$. In case of operational vertices percentage is over 75% from total number of vertices, we talk about linear GSA.

OLC is a sequence of operational vertices of graph-scheme of algorithm. Each OLC α_g has accidental number of inputs I_g^i and only one output Q_g. Formal definitions of OLC, its input and output one can find in [5]. OLC with only one input and one output is called elementary [2].

OLC, outputs of which are connected with the input of the same vertex are called pseudoequivalent operational linear chains (POLC). Such OLCs make the class B_i. All classes are packed into the set $B = \{B_1,...B_I\}$ of POLC classes.

Let GSA contains G elementary OLC α_g that form the set C.

$$R_1 = \lceil \log_2 G \rceil \quad (1)$$

bits are enough for encoding elements of the set C. Number of components in OLC α_g is marked as F_g. Maximum length $Q = \max(F_1,...F_G)$ of linear chain

determines number of bits R_2 in the code for encoding OLC components, where

$$R_2 = \lceil \log_2 Q \rceil. \quad (2)$$

Elements $\tau_r \in \tau$ and $T_r \in T$ are used for encoding elementary OLC and their components accordingly. It being known that $|\tau| = R_1$ and $|T| = R_2$. Encoding of components is performed in natural order, that is

$$K(b_{gi}) = K(b_{gi-1}) + 1, \quad (3)$$

where $g = 1, ..., G$, $i = 1, ..., F_g$.

Each operational vertex $b_q \in E_1$ corresponds to microinstruction MI_q storing in control memory (CM) in the cell with address $A(b_q) = A_q$. Code sharing is obtaining of the address A_q as concatenation of OLC code and its component code [2]. Total width of address is

$$R_A = R_1 + R_2. \quad (4)$$

Structure of compositional microprogram control unit with elementary OLC and code sharing can be used for interpr etation of graph-scheme of control algorithm (Fig. 1). Let us call this structure U_1.

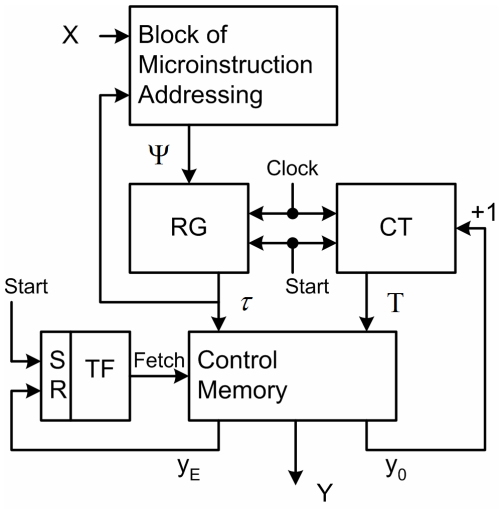

Fig. 1. Structure of compositional microprogram control unit with elementary OLC and code sharing

Block of microinstruction addressing in CMCU scheme realized function of memory excitation for register RG:

$$\Psi = \Psi(X, \tau). \quad (5)$$

When signal Start is coming initial microprogram address is loaded into RG, zero value is loaded into CT, and flip-flop TF is set to "1" that allows reading microinstructions from control memory. There are two additional internal signals: y_0 and y_E. In case of $y_0 = 1$ content of CT is incremented and next vertex of current operational linear chain is addressed. If $y_0 = 0$ then OLC output is reached and BMA prepares address of next OLC using code of current POLC class. Signal y_E is used at the end of microprogram to reset flip-flop TF. The value "0" of TF output stops access to CM.

Asynchronous reset of counter must be controlled by function Start $\vee \overline{y_0}$. Signal $\overline{y_0}$ ensures loading zero value to the CT when transition to another OLC performed.

Number of terms in BMA scheme can be decreased by implementation OLC code transformer into POLC class codes [2]. But such realization demands extra FPGA recourses.

In the article complexity of code transformer is proposed to decrease by additional vertices with pseudoequivalent class codes. Free recourses of embedded memory are proposed for storing additional microinstructions.

III. Main Idea of Proposed Method

In initial GSA the set C_1 contains OLC α_g, which are not connected to the end vertex of GSA. All operational linear chains are divided into classes $B_i \in \Pi_C$ of POLC. Binary code $K(B_i)$ of width R_3 is set to each class B_i, where

$$R_3 = \lceil \log_2 I \rceil. \quad (6)$$

In (6) I is number of POLC classes. After output vertex of each OLC $\alpha_g \in C_1$ additional vertex is added. It contains pseudoequivalent class code $K(B_i)$ of current OLC. For modified OLC encoding R'_2 five bits are enough, where

$$R'_2 = \lceil \log_2 Q' \rceil. \quad (7)$$

In (6) Q' is maximum number of vertices in OLC after their modification, therefore $R'_2 \geq R_2$.

Embedded memory blocks (EMB) in FPGA can be configured for different task performing. So, in Stratix III chip exists next configurations: 16K×8, 8K×16, 4K×32, 2K×64, 16K×9, 8K×18, 4K×36, 2K×72 [4]. Total number of chip contacts is constant value, that's why method modification usage restriction presents. If N_c is memory chip contacts number, then

$$n_1 = N_c - R'_A \quad (8)$$

free contacts of each block can be used for microinstruction generation, where

$$R'_A = R_1 + R'_2. \quad (9)$$

For all output signals realization N_{EMB} memory blocks are used:

$$N_{EMB} = \left\lceil \frac{N+2}{n_1} \right\rceil. \quad (10)$$

In (10) N is number of bits for output signals unitary encoding [2]. Constant «2» takes into account additional

internal variables y_0 and y_E. Total number of unused memory outputs is obtained according (11):

$$n_2 = n_1 * \left\lceil \frac{N+2}{n_1} \right\rceil - (N+2). \quad (11)$$

Address width of OLC component can be increased as a result of additional vertices implementation. In this case only $(n_1 - 1)$ outputs of each block are used for output functions realization. If number of used EMB still the same when number of free memory outputs is decremented, usage of proposed method modification is reasonable, i.e.:

$$\left\lceil \frac{N+2}{n_1} \right\rceil * n_1 = \left\lceil \frac{N+2}{n_1 - 1} \right\rceil * (n_1 - 1). \quad (12)$$

Thereby, condition of reasonability is one of next conditions fulfillment:

$$\begin{cases} R_2' = R_2; \\ \left\lceil \frac{N+2}{n_1} \right\rceil * n_1 = \left\lceil \frac{N+2}{n_1 - 1} \right\rceil * (n_1 - 1). \end{cases} \quad (13)$$

First condition means the same code width for encoding both non-modified and modified OLC components. Second one ensures the same number of used EMB block when codes of non-modified and modified OLC components have different widths. If one or/and two conditions from (13) take place, modification of syntheses method can be done. CMCU structure U_2 is obtained (Fig. 2).

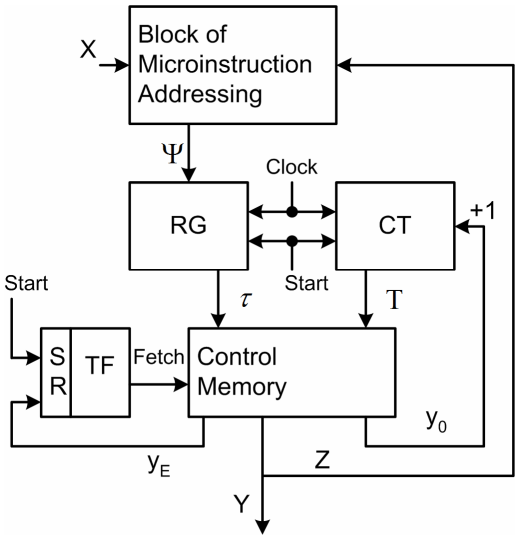

Fig. 2. Structure of compositional microprogram control unit with elementary OLC and code sharing after implementation addition microinstructions

In CMCU U_2 variables $z_r \in Z$, where $|Z| = R_3$, are bits of code $K(B_i)$. Block of microinstruction addressing performed function

$$\Psi = \Psi(Z, X). \quad (14)$$

Other blocks of CMCU U_2 perform corresponding functions to functions of CMCU U_1 blocks. Let us point out that structural elements BMA, CT, RG, TF is realized in LUT-elements, and CM is implemented in embedded memory.

The following method of CMCU U_2 synthesis is proposed in this article:

1. Construction of the sets C, C_1, and Π_C for a GSA Γ.
2. Implementation of additional vertices with pseudoequivalent class codes $K(B_i)$ to OLC α_g.
3. Encoding of OLC, their components and classes $B_i \in \Pi_C$.
4. Construction of the content of control memory.
5. Construction of CMCU transition table and $\Psi = \Psi(Z, X)$ functions.
6. Synthesis of CMCU logic circuit.

IV. Example of Method Using

Let GSA Γ_1 (Fig. 3) be characterized by next sets: $C = \{\alpha_1, ..., \alpha_6\}$ – elementary OLC, $C_1 = C \setminus \{\alpha_5, \alpha_6\}$ OLC without connection to the end vertex, $\Pi_C = \{B_1, B_2\}$ – classes of pseudoequivalent operational linear elementary chains, where $B_1 = \{\alpha_1\}$, $B_2 = \{\alpha_2, \alpha_3, \alpha_4\}$.

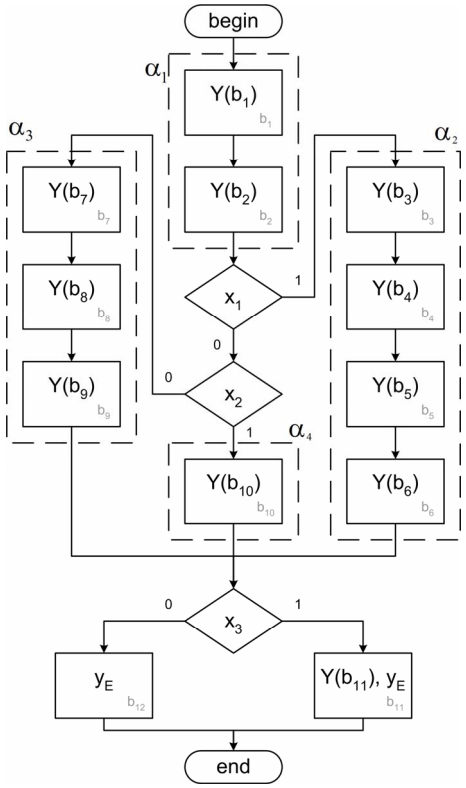

Fig. 3. Initial GSA Γ_1 before implementation of additional vertices with pseudoequivalent class codes

Number of OLC $G = 6$, $R_1 = 3$ bits from the set $\tau = \{\tau_1, \tau_2, \tau_3\}$ are used for their encoding. Maximum length of OLC is $Q = 4$, let us use $R_2 = 2$ variables from the set $T = \{T_1, T_2\}$ for OLC components encoding. Total number of operational vertices is $M = 12$, this number demands $R = 4$ bit of address in CM. For encoding $I = 2$ classes $B_i \in \Pi_C$ of POLC $R_3 = 1$ bit is used.

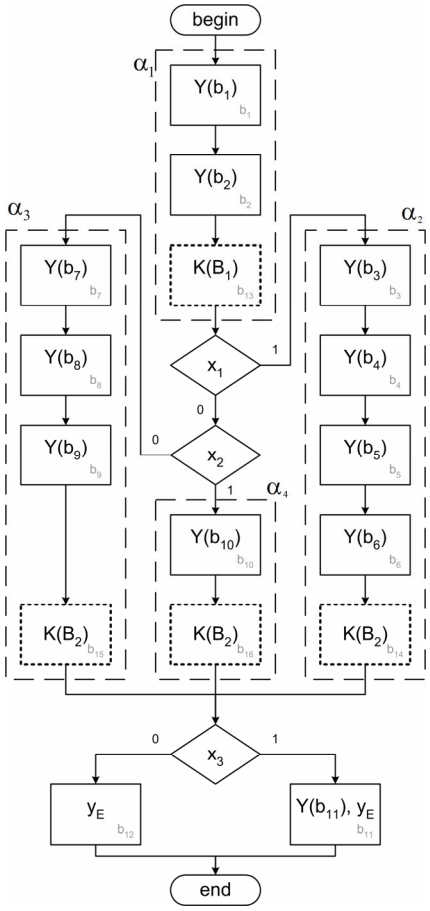

Fig. 4. Initial GSA Γ_1 after implementation of additional vertices with pseudoequivalent class codes

Let us encode OLC $\alpha_g \in C$ and their components in arbitrary manner (3). Addresses $A(b_q)$ of CMCU $U_2(\Gamma_1)$ microinstructions are shown in Table I. Here and after symbol $U_i(\Gamma_j)$ means, that CMCU U_i interprets GSA Γ_j. From Table I one can obtain addresses as concatenation of OLC code and code of component, for example: $A(b_6) = 001011$, $A(b_{10}) = 011000$ and so on. Extra bit is added to the OLC component code according to (6) and (9) because of maximum length of OLC after modification is $Q' = 5$.

TABLE I
ADDRESSES OF CMCU MICROINSTRUCTIONS

$(T_0)T_1T_2$ \ $\tau_1\tau_2\tau_3$	000	001	010	011	100	101
(0)00	b_1	b_3	b_7	b_{10}	b_{11}	b_{12}
(0)01	b_2	b_4	b_8	b_{16}	–	–
(0)10	b_{13}	b_5	b_9	–	–	–
(0)11	–	b_6	b_{15}	–	–	–
(1)00	–	b_{14}	–	–	–	–

Codes of classes $B_i \in \Pi_C$ are set as $K(B_1) = 0$, $K(B_2) = 1$. Microinstruction format of CMCU U_2 in case of $y_0 = 1$ includes fields y_0, y_E, FY, where field FY contains code of microoperation set; and in other case y_0, y_E, FB – code of class $B_i \in \Pi_C$.

Let EMB block contacts be $N_C = 25$ [4], then according to (8), each block has $n_1 = 25 - 5 = 20$ free contacts. Let us suppose number of output functions be $N = 30$. For their realization $N_{EMB} = 2$ blocks of memory are used (10). According to (11) last block has $n_2 = 8$ free contacts after realization of all output functions. Second condition of (13) takes place, modification of syntheses method is reasonable. Contents of CMCU $U_2(\Gamma_1)$ control memory is shown in Table II.

TABLE II
CONTENTS OF CMCU CONTROL MEMORY

$A(b_q)$	y_0	FY		y_E
		FB	*	0
$A(b_1)$	1	$Y(b_1)$		0
$A(b_2)$	1	$Y(b_2)$		0
$A(b_{13})$	0	$K(B_1)$	*	0
$A(b_3)$	1	$Y(b_3)$		0
$A(b_4)$	1	$Y(b_4)$		0
$A(b_5)$	1	$Y(b_5)$		0
$A(b_6)$	1	$Y(b_6)$		0
$A(b_{14})$	0	$K(B_2)$	*	0
$A(b_7)$	1	$Y(b_7)$		0
$A(b_8)$	1	$Y(b_8)$		0
$A(b_9)$	1	$Y(b_9)$		0
$A(b_{15})$	0	$K(B_2)$	*	0
$A(b_{10})$	1	$Y(b_{10})$		0
$A(b_{16})$	0	$K(B_2)$	*	0
$A(b_{11})$	*	$Y(b_{11})$		1
$A(b_{12})$	*	-		1

As one can see from Table 2, if $b_q \in E_1$ is output of OLC $\alpha_g \in C_1$, microinstruction has value "0" in y_0 field and code $K(B_i)$ instead of output function set $Y(b_q)$ in the microinstruction word.

Transitions from outputs of OLC $\alpha_g \in C_1$ are expressed by next system of formulae [2]:

$$B_1 \to x_1 b_3 \vee \overline{x_1} x_2 b_{10} \vee \overline{x_1 x_2} b_7; \qquad B_2 \to x_3 b_{11} \vee \overline{x_3} b_{12}. \tag{15}$$

Such system is the base for CMCU U_2 transition table formation. This table consists of next columns: B_i, $K(B_i)$, b_q, $A(b_q)$, X_h, Ψ_h, h. Their purpose became clear from Table III.

TABLE III
FRAGMENT OF CMCU TRANSITION TABLE

B_i	$K(B_i)$	b_q	$A(b_q)$			X_h	Ψ_h	h
	z_1		τ_1	τ_2	τ_3			
		b_3	0	0	1	x_1	D_3	1
B_1	0	b_7	0	1	0	$\overline{x_1 x_2}$	D_2	2
		b_{10}	0	1	1	$\overline{x_1} x_2$	D_2, D_3	3

Addresses of microinstruction is taken from Table 1. Let us point out, that system of memory excitation functions Ψ includes functions $\{D_1, D_2, D_3\}$. Total number of rows $H_2(\Gamma_j)$ in transition table of CMCU $U_2(\Gamma_j)$ is equal to number of terms in system transition formulae. In our example, $H_2(\Gamma_1) = 5$.

System (15) is formed according to transition table. Fragments of system Ψ can be found from Table III:

$$D_2 = \overline{z_1 x_1}; \qquad D_3 = \overline{z_1} x_1 \vee \overline{z_1 x_1} x_2. \tag{16}$$

For minimization of terms number in (15) classes $B_i \in \Pi_C$ may be encoded with the help of ESPRESSO algorithm, for example.

Realization of logical circuit of CMCU U_2 reduces to implementation of system (16) in base of integrated circuit (FPGA) and realization of control memory on blocks of embedded memory. Modern CAD systems or methods [1, 2] can be used for this purpose.

V. CONCLUSION

Proposed method of OLC modification for compositional microprogram control unit is oriented to LUT-elements decrease in the block of microinstruction addressing. Number of memory blocks in device is the same as for base structure CMCU U_1 with code sharing. Extra clock cycles are used for analysis GSA additional vertices. But at the same time complexity of control unit circuit decreases, that leads to clock signal duration reduction. Conclusion about time characteristics of control unit can be done only for individual case.

Disadvantage of proposed method is in its usage limitation (13).

Scientific novelty of proposed method modification is in usage of POLC classes and free recourses of control memory for LUT-elements number decrease in block of microinstruction addressing. Practical meaning is in chip parameters decrease. It allows realization of device with less cost.

Our future work is directed at development of CAD system for synthesis of control units [5].

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