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NETWORK PROCESSORS DEVELOPMENT CHALLENGE

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В статті виконаний огляд мережних процесорів. Проаналізовані вимоги, що пред'являються до розробок і моделей мережних процесорів.

The convergence of public voice and data networks is speeding up the pace of change in the communications industry. This is leading to increased time-to-market pressure and shorter product lifecycles. Although IP is emerging as the dominant protocol, newly defined IP capabilities, such as Quality of Service (QoS) and Multiprotocol Label Switching (MPLS), require vendors to continually support new applications. As a result, networking products require the same programmability and flexibility that was available in the early CPU-based architectures in order to quickly adapt to emerging standards.

The aim of this paper is to provide a survey of network processors (NPs), which are a new type of special microprocessors intended for networking equipment, mainly switches and routers.

Network processors (NPs) are chips-programmable devices that can process network packets (up to hundreds of millions of them per second), at wire-speeds of multi-Gbps. Their ability to perform complex and fl exible processing on each packet, as well as the fact that they can be programmed and reprogrammed as required, make them a perfect and easy solution for network systems vendors developing packet processing equipment. Network processors are about a decade old now and they have become a fundamental and critical component in many high-end network systems and demanding network processing environments.

Network Processors, emerging on the market today, deliver hardware-level performance to software programmable systems. It allows systems designers to focus on higher-level services and ensures longer product lifecycles [1-3].

A network processor is an application-specific instruction processor (ASIP) for the networking application domain with architectural features and/or special circuitry for packet processing at wire speed. The network processor differs from traditional microprocessors in three ways: 1) the instruction set of many network processors is based on existing RISC processor instruction sets; 2) the network processor’s instruction set contain

special instructions intended for, e.g., bit manipulation, CRC calculation, and search and lookup operations; 3) special hardware function blocks are present to accelerate specific packet processing tasks. In the table 1, we describe the general requirements of network processor [4].

Table 1

The general requirements of network processor

Performance	By executing key computational kernels in hardware, NPs are able to perform many applications at wire speed
Flexibility and programmability	Having software as a major part of the system allows network equipment to easily adapt to changing standards and applications
Fast time to market (TTM)	Time to market has become a critical factor in achieving success with network equipment, it is the time required for system vendor
Serviceability	Users are demanding services such as real-time video, secure private networks and voice over IP, these will require lot of serviceability at the access and edge network elements.

Typical functions performed by network processors are presented in table 2.

Table 2

Typical functions performed by network processors

Lookup and pattern matching	This function compares packet header fields with specific patterns to classify the type of packets
Forwarding	This function is defined as determining the output path for incoming packets.
Access control and queue management	Once packets have been identified and placed in appropriated queues.
Traffic shaping and control	Some protocols or applications require that, as traffic is released to the outgoing wire or fiber.
Data Manipulation	This is where the packet is modified in some way, this could be decrementing the Time To Live (TTL) field in a IP packet.

The abstract model of network processor is depicted in Figure 1. Each network processor is combination of many different elements, that are described in the table 3.

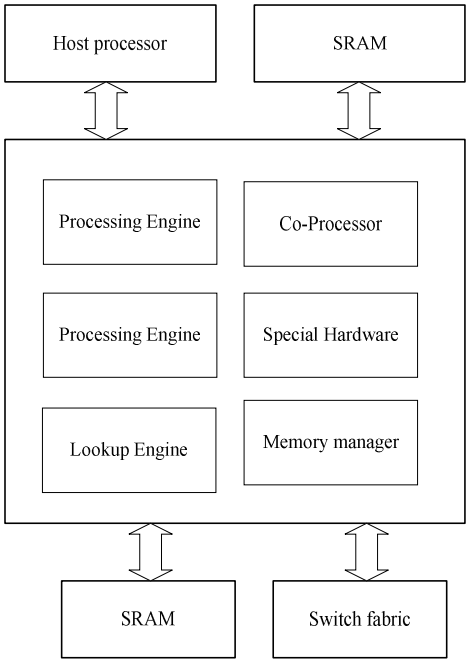

Figure 1. The abstract model of network processor

Table 3

The implementation requirements of network processor

The processing engine	Many network processors are multi-processors, meaning that they are not built as one big RISC processor.
Exploiting parallelism	All network processors are using parallel techniques and pipelining.
NP memory architecture	A critical resource in NPs is the memory architecture. There are three types of memories in NPs including: instruction memory, packet memory, and route table memory.
Dedicated hardware	All network processors incorporate special hardware and integrated co-processors to perform common networking tasks.
Network interface	The most important feature next to a network processor is the network interface.
Software support	Thus far, the considerations were all related to the hardware of the network processor, but of equal importance is software support.

In table 4 we present common approaches in designing NPs.

Table 4

The common approaches in designing NPs

ASIC (application specific integrated circuit)	Any hardwired solution including a microchip that has been designed from scratch for a specific application.
ASIP (application specific instruction processor)	An instruction set processor specialized for a particular application domain.
Co-processor	A hardwired, possibly configurable solution with a limited programming interface.
FPGA (field programmable gate array)	A device that can be reprogrammed at the gate level.
GPP (general purpose processor)	A programmable processor for general purpose computing.
Traditional RISC-based approach architectures	The RISC architectures are the basic infrastructures of many existing NPs.
Special processor architectures	Some NPs use special processor architecture techniques, such as modified co-processor and special functional units to improve their performance.
Massively parallel architectures with modern RISC approach	Some NPs utilize multiple PEs to exploit Parallelism

The information provided in tables 5 describe that all NPs have some kind of special hardware to execute common time-consuming tasks faster and executes special instructions to speed up network processing functions.

Table 5

The architectural comparison for some NPs

NP	Special Hardware	Special Instructions	Layering Support
Agere Payload-Plus	FFP (Fast Patten Processor), ASI (Agere System interface), RSP (Routing switch processor)	For traffic management, QoS and packet modification	L2-4
Intel IXP 1200	Specialized functional unit for hashing and queue management	yes	L2-4
IBM PowerNP	Co-processor to accelerate tree search and frame manipulation	yes	L2-4

Table 5

The architectural comparison for some NPs (Continues)

Motorola C-5	Fabric processor, table lockup unit, and queue and buffer management	yes	L2-7
Ezchip NP1	Four special processors, MAC queue, and search engine	Each TOP(Task Optimized Processor) has its ISA	L2-7
Cisco PFX	16 processor packet forwarding function	yes	L2-4
Cognigine	16 Processing element or reconfigurable communication unit	yes	L2-7
AlchemyAU1xxx	MIPS processor	yes	L2-4
BRECIS(MSP5000)	2 DSP processor	yes	L2-4
Broadcom(SB1250)	2 MIPS 64 bit	no	L3-7
Applied Microcircuit	Packet transform, search, and policy engines	yes (optimized ins.)	L2-4
ClearSpeed	Table lookup engine	no	L2-4
Virtese Sitera	Co-processor for lookup, classification, and queue management	yes	L2-3

Conclusion

In this paper, we introduced the field of network processors by first presenting a description of what network processors are. Subsequently, we described the general, functional, and implementation requirements to such processors must meet. Afterwards, a brief survey of design approaches was discussed in conjunction with a summary of commercially available network processors.

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