The through simulation of devices on the basis of the structural linguistic method

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***Abstract*-The through analysis, synthesis and design of multi-input devices of relay protection and automatics on the basis of the structural linguistic method are considered in the given article. The article shows the development of the steady-state devices in the conditions of variety of input meaningful situations. The article presents methods of further improvement of CAD through design.**

1. INTRODUCTION

The analysis, synthesis and design of multi-input devices of the relay protection and automatics (RP&A) operating with complex objects of control and protection (OCP) in the conditions of variety of input meaningful situations have caused the necessity to apply the structural linguistic (SL) method [1]. Preliminary studies have shown the effectiveness of SL method application to analyze the reasons of unstable operation of RP&A devices of the distribution networks with voltages 6-35 kV. The aim of this article is to investigate the problems of deterministic simulation in accordance with SL method during the through design of devices with specified characteristics. Another aim is to give some ways to improve RP&A devices designed on the basis of multi-core integrated circuits and suggest wider application of SL method in industry.

It is known that the effective development of the devices starts and finishes within the limits of CAD through design. The following stages are used when developing devices in CAD: from an original idea to structural diagrams of improved devices, well-functioning schematic diagrams and programs, then to printed circuit boards and construct and finally to the adjustment of the completed devices. The development of the devices is based on the simulation modeling of device components when signals of the real processes in OCP are sent to the device inputs. It is also based on combined simulation of devices including OCP.

2. THE DESCRIPTION OF SL METHOD

The method is based on the analogy between the structure of objects and the syntax of a language. Objects consist of linked sub-objects similar to phrases and sentences which are made up of words and words in their turn consist of the letters. The flow of real time meaningful information, which is transferred by means of the signal parameters of the input device coordinates, is divided by the information transducers with the threshold output, that is by terminal symbols (TS). The practical creation of TS is based on the methods, which have been justified technically and economically. When we assign the proper names to each elementary information component of TS and to the law how to process it (*P)*, we obtain the opportunity to define the characteristic features typical for any current meaningful situation with respect to permissible meaningful flow of information (to the transient process in the circuit that is the consequence of the emergency situation).

3. THE APPLICATION OF THE SL-METHOD TO CONSTRUCT THE STEADY-STATE DEVICES

The stages of device simulation, according to SL method, are the following: 1) decomposition of the signals of the device input coordinates into the structural information components of TS; 2) construction and analysis of the generalized tree to define the meaningful situations of the known devices; 3) construction of the optimal tree of the steady-state device; 4) verification of the optimal tree operation; 5) synthesis of the principal scheme, the construct of the device.

The simulation of the stages in CAD can be examined on the basis of any RP&A device. Let us take the device including all the levels of hierarchy in relation to the processing of the meaningful information. The example of such a device is the scanner-analyzer of the state of the loop of a circuit zero-sequence (LCZS) [2]. Let us briefly describe the purpose, principle of operation and the device characteristics.

To prove the expediency of SL method application in the theorem "*About the meaningful signal existing in the relay protection systems*" is introduced. According to the theorem, the RP systems operating as a result of perturbation may be transformed into the systems operating as a result of deviation. The feedback in such systems is closed with the help of the meaningful signal *S(t)* (See Fig. 1). The change in signal *S(t)* is proportional to the change in the meaningful states of OCP if the signal were imagined by the operator who would control OCP in manual operation. The following concepts can be referred to the characteristic properties of the meaningful signal *S(t)*: the presence of OCP in normal and other modes of operation, effective compression of the parametric information, graphic representation of any complicated meaningful situation, ease of application the signal for analysis, synthesis and design of simple and hierarchical RP&A devices.

The above properties of the meaningful signal *S(t)* allowed us to unite the corresponding RP&A devices operating separately into the single system of the automatic stabilization of the normal mode of operation (ASNMO) LCZS. The aim of the system operation is to locate the faulty sub-circuit of LCZS in case of the one-phase grounding (OPG) and to provide the system performance in indefinable meaningful situations. The development of the system resulted in new design of selective RP devices as the devices

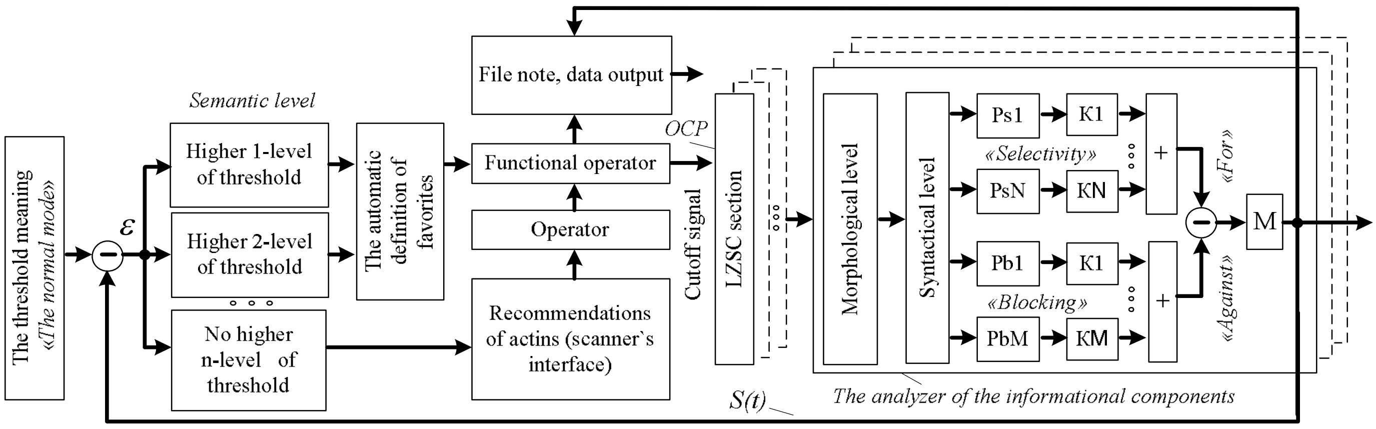

Fig. 1. Structural logical scheme of the "scanner-analyzer".

for the selective search (SS). It also resulted in the necessity to apply devices for self-compensation of OPG currents and alarm circuit recording to realize the search of the OCP faults. The main element of the ASNMO system is the "scanner-analyzer" which is the structural element of a new type of the RP &A "*T-LCZS-1*" terminal. The terminal can be installed in the cell of the voltage transformer and can substitute or complement the RP&A switchboard "The supply line insulation check". Each system device ASNMO forms the completion of the signal *S(t)* by means of the universal algorithm: For–Against "Fig. 1". The group "*FOR*" includes TS, *P* that are responsible for forming the root symbol *S* corresponding to the classical OPG. The group "*AGAINST*" includes TS, *P* that are against forming *S*. The range of the meaningful signal *S(t)* change is within the limits of [0–100%]. Having set the number of the threshold values *P*, for example *Pmax*=98%, we can control the presence and quality of OPG detection, other processes in CZS as well as all high-voltage galvanic coupled machinery. In case of failure (or division) of any part of the ASNMO system, the threshold *Pmax* can be controlled in every device separately. In case there is a lack of information or the latter is greatly distorted in the course of its formation, or given through long time intervals and so on, we can involve the operators. The expert system of the "scanner-analyzer" forms the diagnostic massage about OCP state, the possible cause of the transient process and ways to eliminate this cause.

4. Solution of the Simulation Problems When Applying SL Method

The purposeful transformation of the input meaningful information by means of cascade circuits and programs of device structural blocks imposes certain requirements to the simulation possibilities. In addition to the above-mentioned

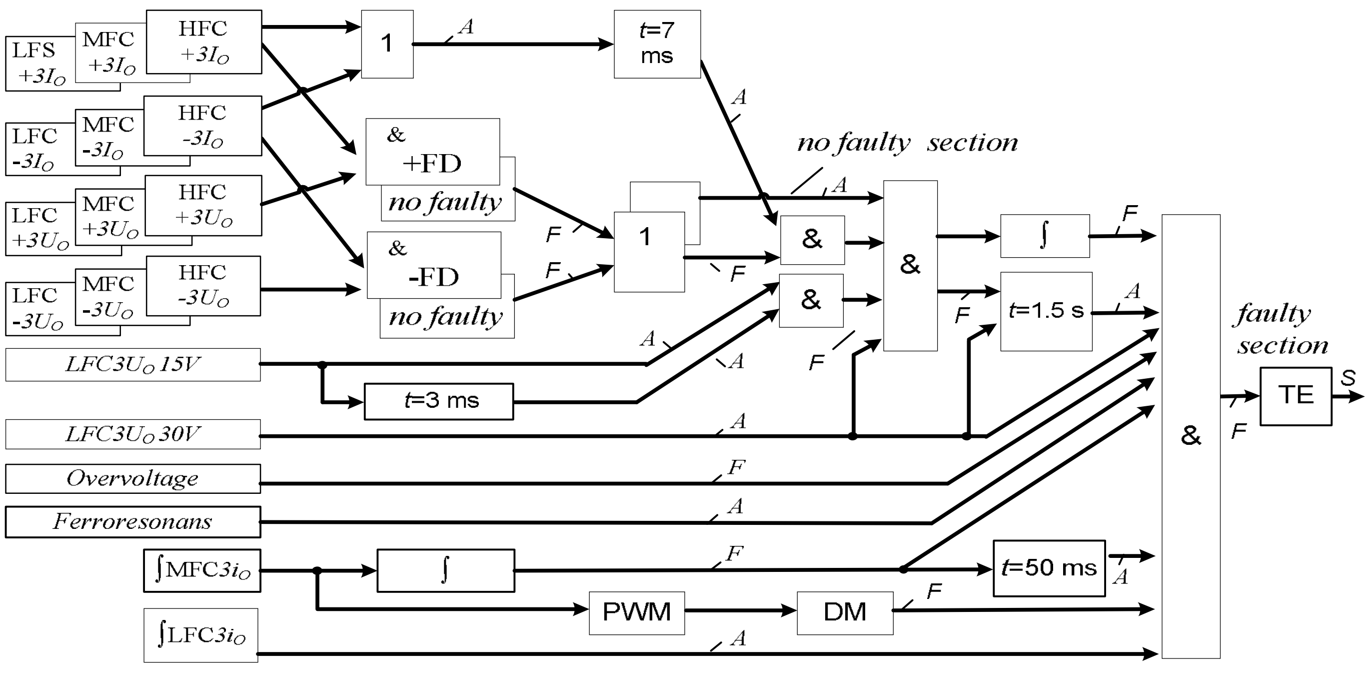

Fig. 2. Structural logical scheme of the "Syntactical level".

requirements we may add the possibility to simulate dynamically within one CAD information transformations by means of morphological, syntactical and semantic levels in consequence. The rapidity of calculation becomes very important.

Fig. 1 shows a multilevel hierarchy of the meaningful information processing, namely the morphological, syntactical and semantic levels according to SL method. Some simulation stages are easy to realize within CAD, but others are not easy to realize. The device simulation showed that CAD "*OrCAD*" is successfully suitable for the majority of SL method stages speaking about all the specified requirements. However, it was difficult to simulate the semantic level and we had to use some other CADs. "*MatLab-Simulink*" turned to be the most effective. Let us consider some problems when simulating by means of SL method.

5. LOW SIMULATION RATE WITHIN CAD

The combination of the hierarchy levels of SL method in one project is unacceptable concerning the simulation time. The reason is that every level operates at different frequencies. Thus, if the frequency of the input information change is 10 kHz (Fig. 2), then the change in the input signal *S(t)* is chosen in the order of 10 Hz. The reduction of input information frequency by 1000 times is equivalent to the compression of the parametric information of signals, which is perfect to construct the system and devices, but not for combined simulation of the hierarchy levels.

The above problem can be solved by decomposition of the project in the following way. The system or the device is structurally divided into the sections realizing the hierarchy levels - the morphological, syntactical and semantic ones. It is usually possible to carry out the division because the number of connections between the levels in the transition points is minimum. Each level is simulated separately at the corresponding frequencies. The transmission of the results from one level to another to complete the project is carried out by the file sources of the signals.

6. SIMULATION OF THE MORPHOLOGICAL LEVEL

The elements of the given level include information transducers (TS), operating at high-, medium-, low-frequency components (HFC, MFC, LFC). TSs include the elements of the galvanic isolation, filters, limiters, drivers, threshold elements (TE). TSs are realized by means of analogue, PWM circuits (perfectly within "*OrCAD*") and by means of microcontrollers (MC) on the basis of the given program. When constructing on the basis of the MC, during the analysis we manage to construct the structural schemes of digital filtration using available *PSpice* -models (ADC, adders and so on). During synthesis we have to use the additional CAD ("*MatLab*") to synthesize filters as there is no suitable tool in "*OrCAD*". The "*OrCAD*" development engineers should be aware of this problem.

The simulation of the principal TS schemes of the known devices within CAD is principally carried out by generating the real signals of the high frequency fault files of the training sample as there are no non-stationary signal components formed by using OCP models. At the given stage, we can find a great number of cases of improper operation of each of the TS component elements. In this case the typical morphological mistakes of TS formation may be divided into groups which must be properly checked - a) the quality and efficiency of operation of the same TS circuit when complex input signals are different; b) interaction of the natural transient oscillations of the filters with current impact effects in case of the arc OPG;

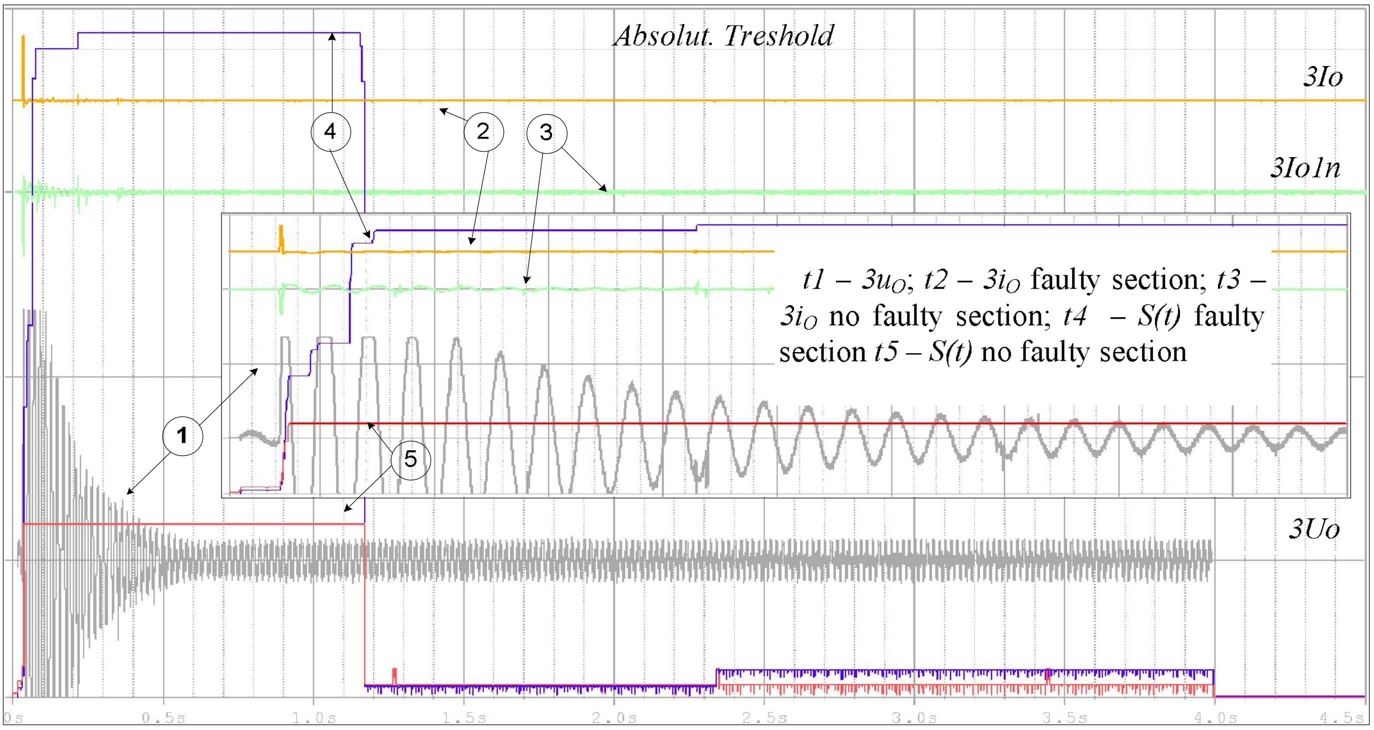

Fig. 3. Simulation of the meaningful situation "*Burst*" LCZS two sections.

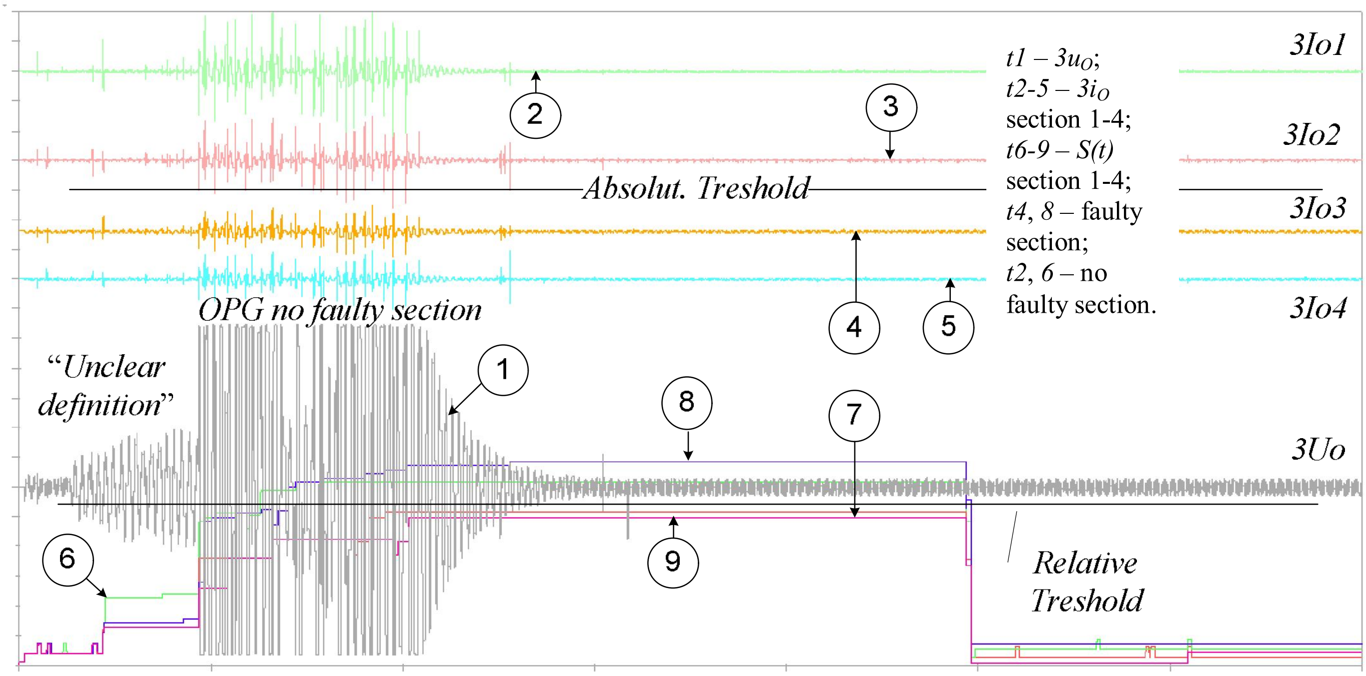

Fig. 4. – Simulation of the meaningful situation LCZS 4 sections. "*Indefinable situation*".

c) the shifting of HFS, MFS band for different OCP. Let us consider the above groups in detail.

As an example, let us analyze the operation of the connected components – an input filter (F)+TE of the certain SS devices (Fig.1, 2) -

a) From the very beginning the SS devices were designed to determine selectively the fault of LCZS section in case of the dead OPG in operating mode of circuit with the insulated neutral. Under existing conditions the regular OPG break down, as a rule, occurs during each half-wave of commercial frequency ω. From the point of view of the response of the connection FLFS+TE the signals of the input coordinates *3uo*, *3io* are similar in case of arc and dead OPG (concerning repeatability, regularity are similar to frequency ω). According to the inventors of the SS devices, the similarity must increase especially when the arc OPG transforms into the dead one because of high breakdown current. The known statistics and the latest OPG monitoring using the fault recorders show that the number of steady-state processes in conditions of OPG at the frequency of ω (the dead OPG) doesn't exceed 1.5-2% in comparison with the number of all OPG but in some circuits the above-mentioned processes can occur very seldom. That is the similarity but not the determinacy of the device structure that helps to operate in case of the arc OPG. Simulation shows that the field of unstable mode of device operation is not limited.

b) The voltage recovery time of the fault phase in the circuit with the resistor-grounded neutral conductor is half cycle-a cycle ω. The interval between the OPG breakdowns is influenced by the individual characteristics of the circuit at the certain moment of its operation as well as by the change in the capacitive current when the modes of circuit operation and user operation changes. Each circuit has its own time intervals between the OPG breakdowns, which differ from the intervals in other circuits, but the parameters of the SS device circuit scheme remain the same. Here we are faced with the problem of choice and adjustment of the SS device parameters according to the circuit characteristics.

c) TS "*LFC3Uo*" contains a lot of information about LCZS and OPG (See Fig. 2). However, it happens that this information is transmitted not to all SS devices. When the information is transferred to TS LFC the additional check of $3u_0$ presence doesn't play an important role.

d) As the arc interval is non-linear, OPG current stops flowing mainly during the first passage through the zero value of HFS of the recharging the circuit phase capacitances (discharge capacitance DHFC+charge capacitance CHFC). Duration of the OPG current flow in this case can be T_{OPG}=1-2 mS (See Fig. 2). When the time T_{OPG} elapses, the character of the transients in the circuit should be related not to OPG but to the stage of recovery of the normal operating conditions of the circuit and this stage does not have the selective phase shifts between LFC $3u_0$, $3i_0$ at ω frequency. How soon the next OPG breakdown occurs depends on the voltage recovery rate in the point of the breakdown (that is on the mode of the neutral grounding). The less the recovery time is, the greater is the probability of the next OPG breakdown. Thus, simulation shows there are practically no selective signals at the frequency ω in conditions of the arc OPG.

e) In different distribution networks DHFC, CHFC can be shifted along the frequency scale, there can be big or slight frequency diversity, DHFC can dominate over CHFC or vice versa. That is why *P* "*FD*" (phase detection) is determined in different ways, which is according to DHFC or according to CHFC or DHFC+CHFC in spite of stating the criteria of selectivity.

f) The qualitative formation of TS requires the reliable separation of LFC $3u_0$, $3i_0$ from the HFC signals. An intensive filtration improves its inertia. In the mode of the arc OPG the impact effect of the MFC $3u_0$, $3i_0$ with the peak amplitude and duration T_{OPG} (See Fig. 2) will excite the natural FLFC oscillations and result into TE operation during T_{FLFC}=*(3-*

$5)\omega^{-1}$. Summation of natural FLFC oscillations caused by subsequent OPG breakdowns depending on the interval between breakdowns can lead to both TE operation and TE non-operation. When TE goes off at the output of FLFC+TE connection, the additional significant phase shift takes place because of by the width pulse modulation. Signals of such character can cause incorrect formation of *P* “*HFC-FD*”.

g) HFC $3u_0$, $3i_0$ can be separated for “*HFC-FD*” by producing an intensive filter. APFC formation in known SS devices is carried out by means of either 2T–shaped notch-filters suppressing *w* frequency when the operating frequency band is 0.5-5 kHz or Bessel’s filters of the third order (0.2-10 kHz) or additionally when differentiating the coordinate $3u_0$ or by using the ferroresonance transformers suppressing frequency w and separating (0.5-5 kHz). To reduce the phase distortion the input filters, as a rule, are produced in the same way. However, firstly, the HFC coordinate oscillation $3i_0$ takes place, mainly, with respect to the zero level, that is, the DHFC, CHFC amplitudes of non fault ZSC sections are much greater than those of LFC $3i_0$. Secondly, the amplitudes of the HFC $3u_0$ oscillation take place with respect to the front of LFC $3u_0$ rise, and they reach the phase value of the circuit which is by one order greater than the amplitudes of DHFC, CHFC $3u_0$. Also, as it is mentioned above, the first half-wave of $3u_0$, $3i_0$ coordinates change should be considered as the impact effect. Thus, for example, HFC-filter excited because of the interference (1 V, 0.2 mS) generates the transient process at the natural frequencies. This process actuates TE, TS and non-selective formation of *P* “*HFC-FD*” during two periods ω. The concept of forming the specified APFC is true mainly for steady-state signals. The specific character of the $3u_0$, $3i_0$ signals reduces sharply the efficiency of the high-quality filters to separate HRC $3u_0$, $3i_0$. Consequently, it is more advisable to take into account the inertia characteristics of the filters, but not the concept of the specified APFC. To synthesize the stable – state devices it is more effective to use the programmed FIR-filters having no feedback between input and output. Consequently, the latter have the linear FFC and don’t store the previous information for a necessary period of time.

Having summarized the results of the morphological level simulation, we can say that the standard SS devices functioning at LFC $3u_0$, $3i_0$ in the conditions of the resistor grounded neutral should be applied to circuits where it is possible to guarantee the transition of the first OPG breakdown into the dead OPG if the active component of OPG current increases. It is natural that under existing conditions the total OPG current mustn’t damage the phase-to-phase circuit insulation and the total technical and economic index of the circuit operating mode must meet requirements of the industrial engineering organization. It is clear that the above-mentioned restrictions are not easy to implement, consequently, the application of the resistor-grounded neutral itself is rather restricted. The same concerns the circuit with an insulated neutral the application of which is much more restricted.

7. SIMULATION OF THE SYNTACTICAL LEVEL

The analysis of the morphological level allowed us to show the number of essential disadvantages of the standard SS device modes. The number of these disadvantages is rather big to cause the unstable mode of device operation. The results of

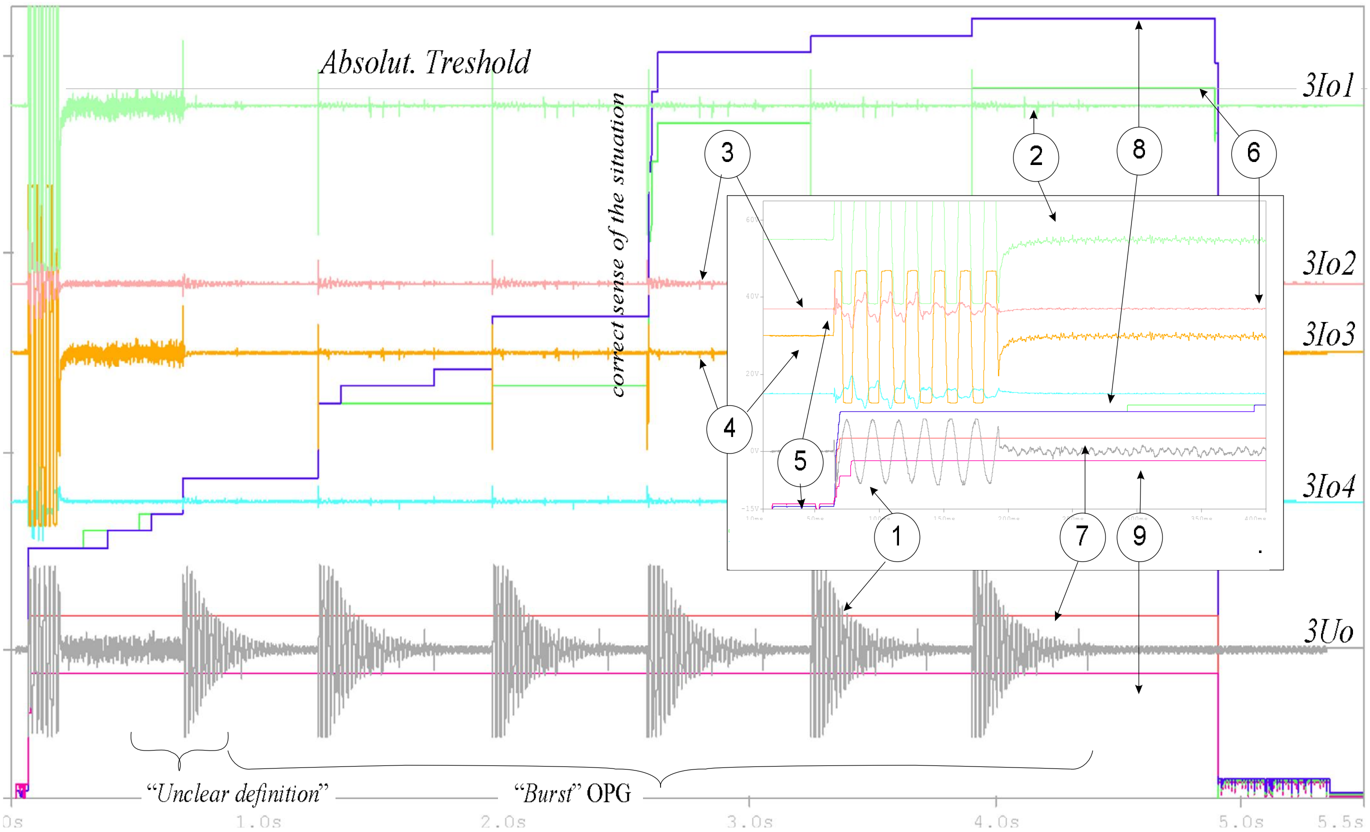

Fig. 5. – Simulation of the meaningful situation LCZS 4 sections. “*Indefinable situation*”. *t1 – $3u_O$*; *t2-5 – $3i_O$* section 1-4; *t6-9 –S(t)* section 1-4; *t4, 8* – faulty section; *t2, 6* – no faulty section.

the synthesis show that the simulation of the automatic circuit-breakers of the syntactical level within the "*OrCAD*" according to SL-method may be successfully carried out under conditions of the device realization on the basis of CPLD (logical elements, VHDL-language). Such realization is suitable and even preferable because the level mainly consists of the great number of the sections of the logical transformation of information functioning in parallel and this level requires a high speed of real time transformation which can't be realized properly by MC.

In case of level realization with the help of MC, the simulation within the "*OrCAD*" is impossible because there are no models of MC calculator and corresponding tools. The development engineers of "*OrCAD*" should be aware of this because the calculator of the latest MC is presented in VHDL-language. Thus, for example, in CAD the "*Proteus*" realizes the through simulation of analogous and constructive parts of the different MC-calculator. Within the CAD "*MatLab-Simulink-Stateflow*" the development of the elements of the program in C-language is supported and automatically formed. MC of the company "Texas Instruments" is simulated too. Unfortunately, other producers are not supported. In "*MatLab*" the development of the morphological level during the analogous and PWM realization is complicated; moreover, the device construction is not developed.

8. Simulation of the semantic level

The realization of the level within CAD "*OrCAD*" is very difficult. The reason is that there are no necessary models and corresponding tools and there arises the problems of optimization and speed of the calculation. For example, the quantity, efficiency and simplicity of realization when choosing TS, *P*, *S(t)*, diagnostic massages are all subject to optimization. Let us consider the tasks of simulation.

a) The first task is the choice of values of the weight factors to apply the rules *P*, which allows to define gradations of the meaningful signal *S(t)* (See Fig.) distinguishing the current meaningful situation from the given one (100%). The task is solved within the "*OrCAD*" by means of the model construction formed into in the hierarchy blocks. However, when it is necessary to use additional TS, *P* on the previous levels - morphological and syntactical, it becomes necessary to carry out a new simulation for these levels and only then for the semantic level. Thus, in case of optimization, the decomposition of the general project is difficult to organize and is time-consuming.

b) The second task is to formulate the of P_{REL} rules of the relative criteria of comparison of the meaningful signals *S(t)* from each faulty OCP section (See Fig. 1,2). To synthesize P_{REL} it is necessary to simulate SS devices not only of faulty and non faulty OCP sub-circuits as it was done during the synthesis of the known SS devises but to simulate three or four SS devises at least. The task of simulation of ASNMO LCZS sub-circuits is to define the order of preferable disconnections when there is the "*Indefinable situation*" and "*Unclear definition*" or several preferences. The formation of automatic control of P_{REL} thresholds, the automatic control of majority determination of the preferences and so on is carried out by means of construction using the elements available in "*OrCAD*". Consequently, the simulation is carried out within the limits of the structural scheme of automatic control constructed by using not the programming language of realization of the level in a device but another language, that is, the (PWM, electrical) language.

c) The task is solved in practice. The simulation of several SS devises in one project complicates the organization of the working place when it is necessary to change the sources of the input signals preliminary prepared at the previous levels of the hierarchy. It is necessary to note that is case of simultaneous simulation of several devices, "*OrCAD*" supports the list of connections, but it takes a lot of time to calculate and the main point is that the calculation stability (the method of Newton-Rawson) significantly worsens.

d) The third task is the construction of the semantic automatic control to take a final decision to disconnect preferences, to choose and fill in the textual and diagnostic massages, to use the file of events and also to take decision in case of "*Indefinable situation*". The special feature of the task is not to take into account the connection of the semantic automats operation with the time axis. The automatic control is realized mainly by means of the programming. Its construction in "*OrCAD*" is rather ineffective. In this case it is necessary to transfer ("*MatLab-Simulink-Stateflow*") to CAD. When realizing the task on the basis of the MC and with the help of both the inserted operational system and the graphic shell, the simulation reduces to the debugging of the operational program of the MC on C-language for PC. The above mentioned solution of the simulation problem minimizes expenditures before starting the device realization and forms the model of the device to work with PC. However, the cost of the MC components is growing rapidly.

CONCLUSIONS

1. It is possible to realize effectively the purposeful analysis, improvement, device design and the organization of the working place of designers on the basis of SL-method. It is especially important for devices on the basis of multi-core integrated circuits.

2. The through design of the device on the basis of SL method shows the discontinuity of the simulation stages, preparation of the design specifications in spite of positioning of the certain CAD as the CAD of the trough design and it also shows the ways of further CAD improvement. In spite of the significant CAD development, the organization of working place of a designer is, unfortunately, carried out on the basis of CAD, maintaining the definite programmable integrated circuits or real electronic components.

3. The following devices of ASNMO LCZS system have been developed within the CAD "*OrCAD*", "*MatLab-Simulink-Stateflow*": the device of the selective search "*VCR-SS-1*", 8-channel high frequency breakdown recorder "*P-SS-1*", the terminal of the RP&A "*T-LZSC-1*".

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