DESIGN OF MOORE AUTOMATON ON THE LINEAR FLOW-CHART

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Abstract

Kovalyov S.A., Barkalov A.A. (BT-95g), Samir Nahlavy. Design of moore automaton on the linear flow-chart. The method of Moore automaton's synthesis on the flow-chart with big amount of operational nodes is discussed. The method is based on the forming of the linear sequences of states and special encoding of the states, That permits to replace the register of the automaton memory by the counter and to decrease the number of LSI circuits in the automaton circuit. The main tasks to solve for design of the circuit on the programmable logic devices are discussed. An example of the logic circuit's synthesis in PLA and ROM basis is shown.

Introduction

The constant progress in the microelectronics has leaded to the development of the wide spectrum of the very large scale integrated circuits, in particularly the programmable logic devices (PLD) [1], such as programmable logic arrays (PLA), programmable array logic (PAL), programmable ROMs. Now this basis is the main one for synthesis of the logic circuits of the automata, for example control units (CU) of the digital systems [2]. One of the main problems in the design of the CU in the basis of PLD is the minimization of the VLSI in the circuit of the CU [3]. In this article the tasks are discussed which are actual in the synthesis of the automata on the linear flow-charts and the ways of their solving.

Base structure of Moore automaton and main definition

Let we have flow-chart $\Gamma = \Gamma(B,E)$, where B is the set of nodes(initial, final, operational, conditional) and E is the set of the arcs. The sets of microoperations $Y_t \subseteq Y=\{y_1, \dots, y_N\}$ are written in the operational nodes $bq \in B$, the elements of the set of logical conditions $X=\{x_1, \dots, x_L\}$ are written in the conditional nodes $bq \in B$. Let us name the flow-chart Γ the linear flow-chart if the amount of the operational nodes is not less than 75% from the general number of the nodes. This peculiarity of the algorithm may be taken into account for simplification of the system of excitation functions of the memory [4]. Let flow-chart Γ has been marked by the

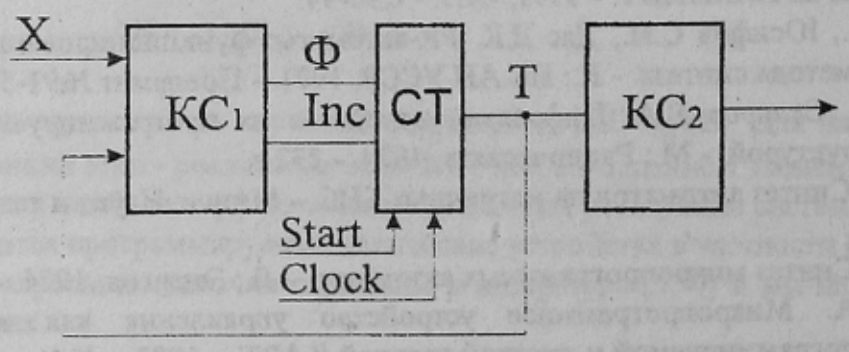

Figure 1. The structure of the Moore C-automaton

states of the Moore automaton S(Γ), which belong to the set A={a_1, ... , a_M}.
Let us introduce the following definitions.

Definition 1. The linear sequence of the states(LSS) of the flow-chart Γ is the finite cortege of the states β_g, such than for any pair of the states $a_{g_i}, a_{g_{i+1}}$, where i is the number of the component of the cortege β_g, there is transition $<a_{g_i}, a_{g_{i+1}}>$ between the states S(Γ).

Definition 2. The state $a_m \in A^g$, where A^g is the set of the states from the LSS β_g, is named as the input of the LSS β_g, if there is transition $<a_s, a_m>$ of the automaton S(Γ) and $a_s \notin A^g$.

Definition 3. State $a_m \in A^g$ is named as the main input of the LSS β_g, if a_m is the initial state of the automaton or a_m is the input of the LSS β_g, which transitions determine the sequence of the logical conditions with last element equal to zero.

Definition 4. State $a_m \in A^g$ is named as the output of LSS β_g, if there is unconditional transition $<a_m, a_s>$, where $a_s \notin A^g$, or there are transitions from state a_m in the states $a_s \in A^g$ with numbers in the LSS β_g less than the number for the state a_m.

The method of synthesis

Let the partition π_β of the states on the classes A^1, ... , A^G has been obtained for the flow-chart Γ such that each class corresponds to the single LSS α_g, and let for each LSS such encoding of the states has been executed that the condition (1) is satisfied for any pair $<a_{g_i}, a_{g_{i+1}}>$, where

$$K\left(a_{g_{i+1}}\right) = K\left(a_{g_i}\right) + 1 \qquad (1)$$

Here $K(a_m)$ is the code of the state a_m ($m=g_i, g_{i+1}$) with the amount of bits $R=]\log_2 M[$.
In this case the register of the memory of the automaton S(Γ) may be replaced by the counter CT and the structure of the automaton circuit is depicted on the Fig.1. Let us name such automaton as C-automaton.
C-automaton operates in the next order. Accordingly with the signal Start the zero is written in the counter CT , this code corresponds to the initial state $a_1 \in A$. In the instant of time t the code of the state $a_m \in A^g$ is in the counter. If state a_m is not the output of the LSS ЛПС β_g, then circuit KC1 forms the signal Inc and after arriving the synchronization signal Clock the

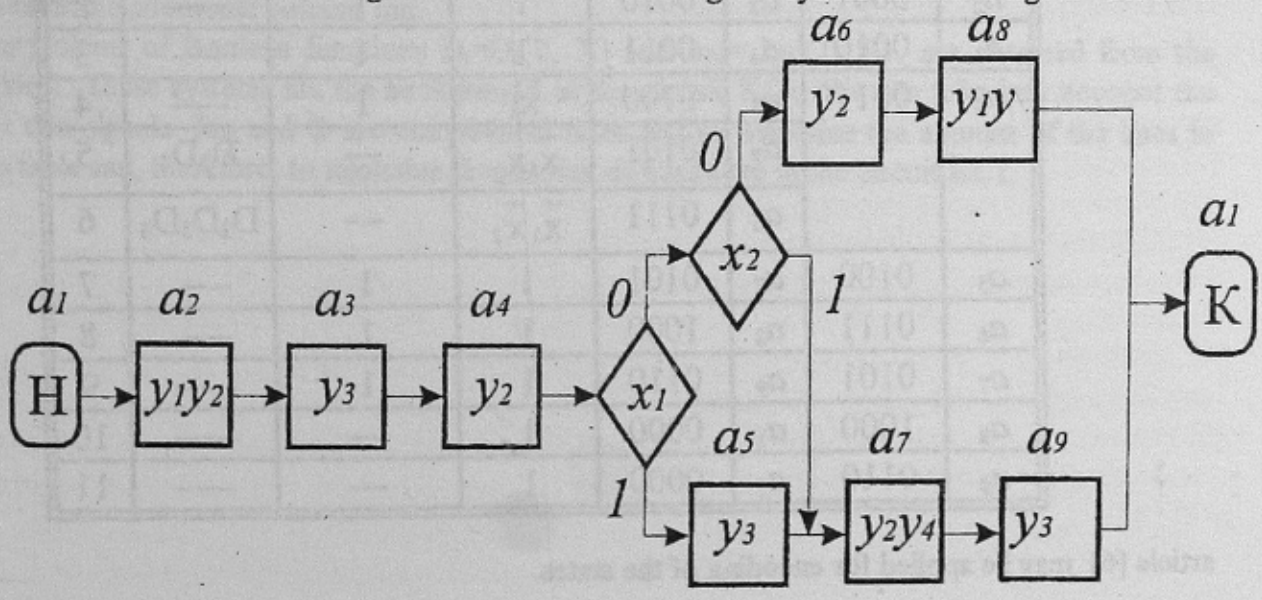

Figure 2. The marked flow-chart Γ_1

increment operation is executed on the content of CT to satisfy the condition(1). If a_m is the input of the LSS α_g, then circuit KC1 forms the excitation functions $\Phi=\{\varphi_1, \dots, \varphi_R\}$ and the code of the state a_s, such that condition (1) is not satisfied for the pair $<a_m, a_s>$. The operation is breaking down if the final state of the automaton has been reached.

The tasks of the synthesis of the automaton with counter have been discussed in the article [4], but they deal with the small scale integrated circuits. The appearance of the PLDs awakes the necessity of the development of the methods of C-automata design with are oriented on this modern basis and on the customized array VLSI [5].The fig.1 depicts the structure of the Moore C- automaton but the same organization may be used for Mealy automata, PR-automata [6] .

Apparently that peculiarities of the each class of automata lead to the peculiarities in the algorithms of synthesis and optimization of hardware in the logical circuits of the automata. To apply the CAD-tools for synthesis of the C-automaton it is necessary to solve the following problems:

1. The formation of the partition π_β of the set of the states A on the classes corresponded to the LSSs and satisfied to the conditions:

$$A^g \cap A^i = \varnothing \quad (i \neq g,\ i,g \in \{1,\dots,G\});$$
$$A^1 \cup A^2 \cup \dots \cup A^G = A; \qquad (2)$$
$$G \to \min.$$

The last from these conditions is oriented on the minimization of the amount of the transitions of automaton, the first from these conditions is oriented on the minimization of the amount of the states. To solve this problem they can use the methods from the work[6] with some modification.

2. The optimal encoding of the states satisfied to the condition (1). In this case the amount of the DST lines with zero excitation functions is increasing. The modified methods from the

Table 1. The direct structural table of the C-automaton $S(\Gamma_1)$

a_m	$K(a_m)$	a_s	$K(a_s)$	X_h	Inc	Φ_h	h
a_1	0000	a_2	0001	1	1	—	1
a_2	0001	a_3	0010	1	1	—	2
a_3	0010	a_4	0011	1	1	—	3
a_4	0011	a_5	0100	x_1	1	—	4
		a_7	0101	$\bar{x}_1 x_2$	—	D_2D_4	5
		a_6	0111	$\bar{x}_1 \bar{x}_2$	—	$D_2D_3D_4$	6
a_5	0100	a_7	0101	1	1	—	7
a_6	0111	a_8	1000	1	1	—	8
a_7	0101	a_9	0110	1	1	—	9
a_8	1000	a_1	0000	1	—	—	10
a_9	0110	a_1	0000	1	—	—	11

article [6] may be applied for encoding of the states.

3. The transformation of the C-automaton's structure oriented on the optimization of the

Table 2. The contents of the ROM of the circuit KC2

Address	Contents	a_m	Address	Contents	a_m
0000	—	a_1	1000	y_1y_3	*
0001	y_1y_2	a_2	1001	—	*
0010	y_3	a_3	1010	—	*
0011	y_2	a_4	1011	—	*
0100	y_3	a_5	1100	—	*
0101	y_2y_4	a_7	1101	—	*
0110	y_3y_5	a_9	1110	—	*
0111	y_2	a_6	1111	—	*

hardware amount. To achieve this aim the methods of the structural reduction and the algorithmic methods from the article [6] may be used after some modification to the peculiarities of the C-automaton.

Example of application of proposed method

Let us discuss the example of the Moore C-automaton's synthesis on the linear flow-chart Γ_1 (Figure 2) without the details of the methods of the above mentioned tasks' solving. There are for flow-chart Γ_1 $X=\{x_1, x_2\}$, $Y=\{y_1, \dots, y_5\}$, $A=\{a_1, \dots, a_9\}$, $M=9$, $R=4$. The set of LSS is $\pi_\beta=\{\beta_1, \beta_2\}$, where $\beta_1=<a_1, a_2, a_3, a_4, a_5, a_7, a_9>$, $\beta_2=<a_6,a_8>$, the states a_1, a_6 are the main inputs of LSSs; the states a_1, a_6, a_7 are the inputs of LSSs; the states a_8, a_9 are the outputs of LSSs.

Let us encode the states of automaton in the following manner: $K(a_1)=0000$, $K(a_2)=0001$, $K(a_3)=0010$, $K(a_4)=0011$, $K(a_5)=0100$, $K(a_7)=0101$, $K(a_9)=0110$, $K(a_6)=0111$, $K(a_8)=1000$. The combinational circuit KC1 is described by the direct structural table (Table 1), which contains the additional column Inc.

The systems of Boolean functions $D_r=D_r(T, X)$ and $Inc= Inc(T, X)$ are obtained from the Table 1. These systems are the background of the circuit KC1. We can take into account the fact that signals Inc and Φ are complement ones and to minimize the amount of the lines in this table and, therefore, to minimize the amount of hardware in the circuit KC1.

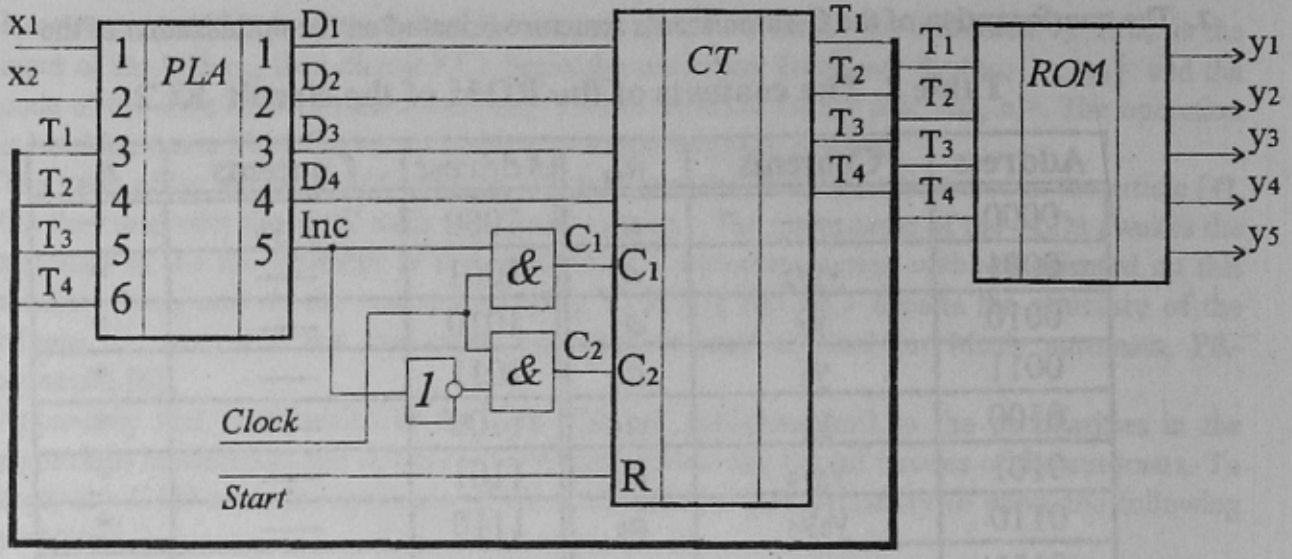

Figure 3. The functional circuit of the C-automaton $S(\Gamma_1)$

The circuit KC2 could be implemented on the ROMs, in this case the code $K(a_m)$ is the address of the word of the ROM with the set of the microinstructions Y_t from the operational node of the initial flow-chart Γ marked as the state a_m (Table 2).
The functional circuit of the C-automaton $S(\Gamma_1)$ is shown on the Figure 3, where the circuit KC1 is implemented on PLA, circuit KC2 is implemented on the ROM.

Conclusion

The research work of the authors shows that the application of this method for the linear flow-charts is always very useful. The gain respectively the automata with the register is increasing with the increasing of the part of the operational nodes in the flow-chart.

Reference

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