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APPROACH OF REALIZATION OF COMPOSITIONAL MICROPROGRAM CONTROL UNIT WITH COMMON MEMORY

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One of the methods of realizations control units as a digital systems is using of the model compositional microprograming control unit (CMCU) [1,2]. This device is ideally approaching for realization with using modern VLSI type FPGA [3], where there are means for realization of any logic and built-in blocks of memory [1]. During the time at mass production products electronic is the industries on-former.

Widely used custom-made circuits type ASIC (Application Specific Integrated Circuit). In this case for realization circuit control units using custom-made matrixes, based on ideas distributed logic. In the present time in literature methods, directed oriented on this basis practically are absent. The present state explains the method of synthesis CMCU with common memory on custom-made matrixes and analysis the ways of reduction area of the chip, borrowed it's logical circuit.

The purpose of research is realization of logical circuit control unit on custom-made VLSI at interpretation of linear control algorithm.

Task of the research is development synthesis CMCU with common memory, allowing to reduce the area custom-made matrix in his logical circuit. At this approach the control algorithm presented in the form of graph circuit algorithm (flow-chart).

Let initial (flow-chart) has initial vertex b_O, final vertex b_E, the set of the operational vertices is B_1 and the conditional vertices set is B_2. In the vertices $b_q \in B_1$ enter for microcommands $Y(b_q) \subseteq Y$, where $Y=\{y_1,\ldots..,y_N\}$- the set of microcommands. In vertices $b_q \in B_2$ is written down in the set of the elements of logical conditions $X=\{x_1\ldots\ldots.,x_2\}$.Vertices flow-chart are connected by arches $<b_t,b_q>$, forming the set an arch E. Let's enter a number of definitions [1,2], necessary for the further statement material.

First Definition: operational linear object (OLO) named final sequence operational vertices $\alpha_g =\{b_{g1},\ldots.,b_{gfg}\}$, such that for any pair of the next component vector α_g exists an arch $<b_g,b_{gi+1}> \in E$.

Second Definition: Input of (OLO) α_g refers to vertex b_q D^g, where the set of vertices entering in OLO α_g, such that $b_t=b_o$ or $bt \in B_2$ or $bt \in O^g$.

Third Definition: Inputs OLO α_g refers to verex $b_q \in D^g$, such that exist an arch $<b_t,b_q> \in E$, where $b_t=b_E$ or $b_t \in B_2$ or $b_t \notin D^g$.

Any OLO α_g can has more than one input, let's designate j input OLO α_g like I_g, every OLO has only one output O, entering in the set $O(\Gamma)$ outputs OLO flow-chart.

Let for the flow-chart generated the set of OLO $C=\{\alpha_1,\ldots., \alpha_G\}$, satisfying conditions

$$D^i \cap D^j=0 \quad (i \neq j; i,j \in \{1,\ldots..,G\});$$
$$D \cup D \cup \ldots\ldots. \cup D^G=B1; \qquad (1)$$
$$G \to \min$$

At performance of conditions (1) every vertex $b_q \in B_1$ enters exactly one OLO $\alpha_g \in C$, the number which is minimal. Let $(b_q) \in B_1$ and having

$$R_A=[\log_2 M] \qquad (2)$$

Categories, where the condition was satisfied

$$A(b_{gi+1})=A(b_{gi})+1 \qquad (3)$$

Where i $\in$ $\{1,\ldots,F_{g-1}\}$ $\in \{1,\ldots,G\}$. Such mode corresponds natural addressing microcommand [2], corresponding the operational vertices flow-chart. Let's name the flow-chart, if the condition satisfied

$$M/G \geq 2 \qquad (4)$$

That is the number of operational vertices would twice exceed the number of OLO.
In this case for interpretation the flow-chart it is possible use the model of CMCU with common memory [2], designated in the further symbol U_1 (Fig. 1).

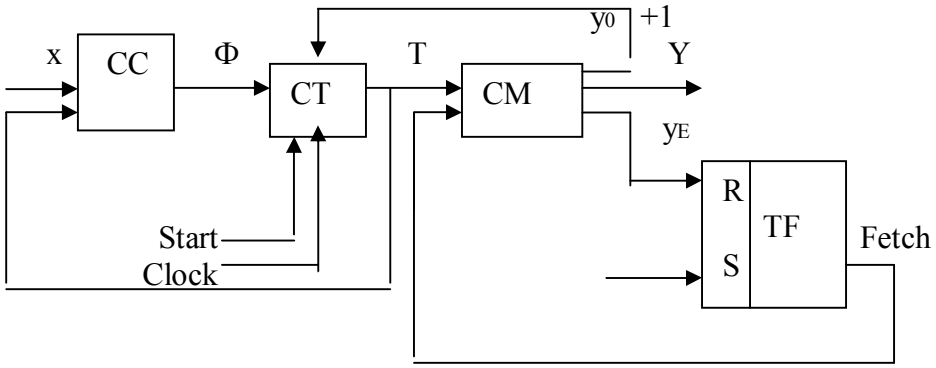

Figure 1 - The structural circuit CMCU with common memory.

This device functions as follows: on signal Start in the counter CT loaded 0 address, the first microcommand of microprogram, corresponding to the flow-chart. Simultaneously the trigger samples TF established in individual state(Fetch=1). The next microcommand MK choose from control memory CM. If this MK corresponds to vertex $b_q \neq O_g$, for simultaneously with the set of microoperations $Y(b_q)$ formed variable y_0=1.if y_0=1, those content CT increase by 1 on the signal Clock. This mode corresponds to (3) that is transition occurs inside of some OLO $\alpha_g \in C$. If $b_q=D_g$, those variable y_0=0 in this case implements the system of input combinational circuit CC functions of the counter CT :

$$\Phi=\Phi(T,X) \qquad (5)$$

It is necessary for loading in CT address input for some OLO. The address enters to CT on signal Clock. If an arch $<b_q,b_E> \in E$, where b_E - final vertex of the flow-chart, those formed variable y_E =1. If y_E =1, thus trigger TF established in zero state (Fetch=0). In this case samples of microcommand from CM is ended, and CMCU will terminate.

Obviously, CMCU is automaton Moore, as output signals y_0,y_E and Y depends only on the contents of CT. Thus the address of microoperations can showing like code of the state automata. However in the difference from classical automaton Moore, memory CMCU is realized on the counter. Thus CMCU with common memory is more optimal then basic structure of compositional unit.

Literature

[1] Barkalov A.A., Titarenko L.A. Synthesis Of Operational And Control Automata. – Donetsk: Unitech, 2005. – 256 pp.

[2] Smith M. Application – Specific Integrated Circuits. – Boston: Addison Wesley, 1997. – 836 pp.

[3] Baranov S. Logic Synthesis For Control Automata. – Boston: Kluwer Accademic Publisher, 1954. – 312 pp.